

eCOG1kG Microcontroller Product Brief

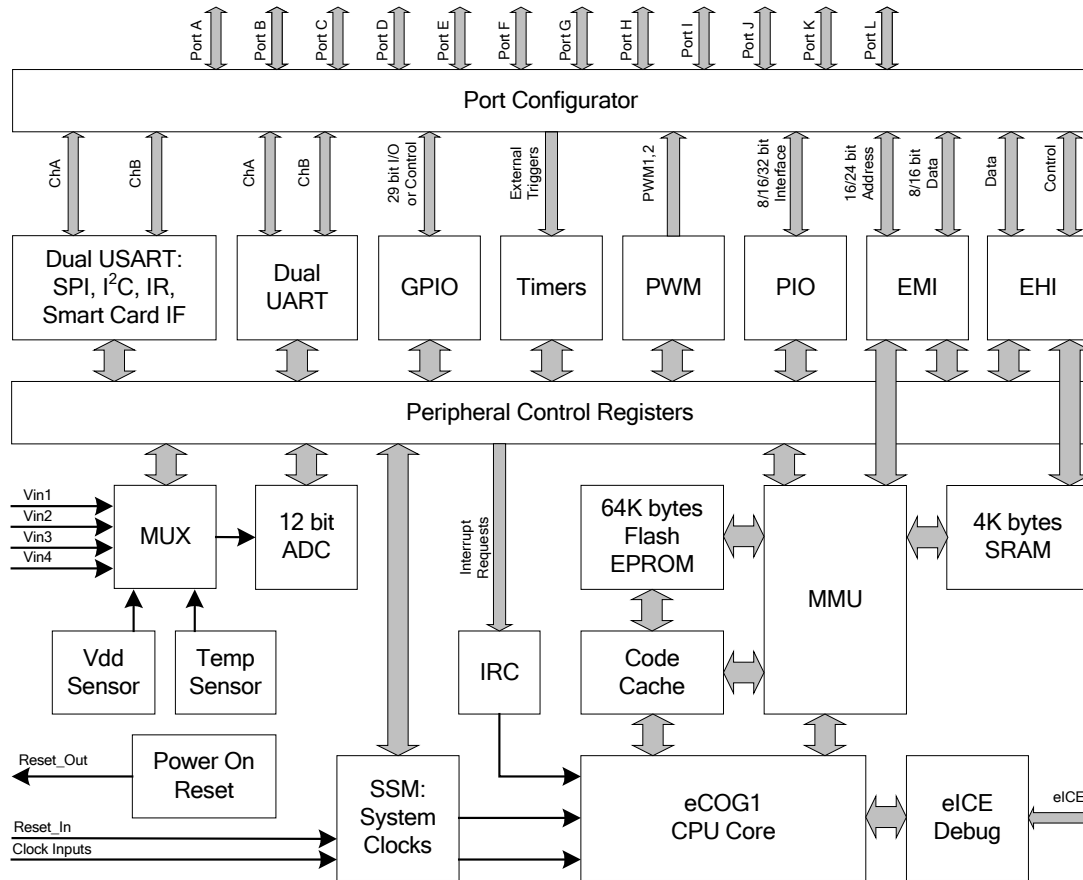


The **eCOG1kG** is a low-power microcontroller, based on a 16-bit Harvard architecture, with a 24-bit linear code address space (32Mbyte) and 16-bit linear data address space (128Kbytes). The device is highly configurable and is available in a 128-pin LQFP package. Comprehensive Development and Evaluation Kits are available. All are fully supported by Cyan's free integrated development environment, **CyanIDE**, which includes automatic peripheral configuration and an unrestricted ANSI C Compiler.

The eCOG1kG is a fully RoHS compliant replacement for the eCOG1k.

- ◆ 0 to 25MHz CPU core
- ◆ Single 3.3V supply
- ◆ Powerful arithmetic operations
- ◆ Barrel Shifter
- ◆ Harvard Architecture
- ◆ Built in Emulator (eICE)
- ◆ Low power operation
- ◆ 64Kbytes FLASH memory
- ◆ 4Kbytes SRAM
- ◆ Memory Management Unit
- ◆ Power-saving code cache
- ◆ Code security feature
- ◆ External Host Interface
- ◆ External Memory Interface
- ◆ Fast Vectored Interrupts
- ◆ Dual UART
- ◆ Dual USART
 - ◆ SPI
 - ◆ I2C
 - ◆ Smart card interface
 - ◆ Infra-red link support
- ◆ 4 channel 12-bit ADC
- ◆ Temperature Sensor
- ◆ Supply Voltage Sensor
- ◆ Power-On Reset
- ◆ 5 Multi Purpose Timers
 - ◆ Clock timer
 - ◆ 2 x counter / timer
 - ◆ 2 x PWM timer
- ◆ Capture timer with 6 inputs
- ◆ Watchdog Timer
- ◆ Long Interval Timer
- ◆ 88 digital I/O pins
- ◆ Parallel I/O ports
- ◆ Up to 29 GPIO pins
- ◆ 25MHz from watch crystal

eCOG1kG block diagram



CPU Core

- 16-bit 25MHz core.
- Harvard architecture.
- 32Mbyte code address space.
- 128Kbyte data address space.
- Vectored interrupts.
- Full ICE debug support.

MMU

- Performs logical to physical address translations.
- Translators for internal SRAM, flash, and external memory devices for both code and data accesses concurrently.
- Up to two concurrent translations to external devices from code space logical addresses.
- Up to three concurrent translations to external devices from data space logical addresses.
- Programmable wait state generation.
- Translations are prioritised to allow overlapped translations.

Flash Memory

- 64Kbytes (32K x 16 bits).
- Organised into multiple sectors.
- Can be mapped into both code and data spaces.
- Global and sector write protection.
- Simple programming via eICE or in-system via CPU.

Code Cache

- Increases execution speed.
- Reduces power consumption.
- Provides a large number of address breakpoints by locking BRK commands in the cache.

Static RAM

- 4Kbytes.
- Can be mapped into both code and data spaces.

External Memory Interface (EMI)

- 8 or 16-bit data bus.
- 16 or 24-bit address bus.
- Multiplexed address/data for 16-bit data bus.
- External devices can be mapped into both code and data space.
- Supports SRAM (bus) and SDRAM interface modes.
- Flexible timing parameters.
- Supports up to 256Mb single data rate 16-bit wide SDRAM including auto and self refresh.
- Supports low power SDRAM suspend/standby mode.

External Host Interface (EHI)

- Provides an interface to an external host processor or FIFO.
- Supports both DMA and memory mapped peripheral modes.
- Interrupts on transfer complete.

DMA Mode:

- Master and slave mode operation.
- 16/32-bit data bus.
- Request & Acknowledge control lines.
- Configurable master mode timing.
- DMA into internal SRAM.
- Circular and linked list buffer models.

Memory Mapped Mode:

- Selectable block size:
256 x 16-bit data or 8 x 32-bit data.
- Three control lines: chip select, read/write direction and wait.

DUARTs

- Dual UART module.
- Two asynchronous double-buffered serial ports.
- 5, 6, 7, or 8 data bits.
- 1, 1.5 or 2 stop bits.
- Even, odd or no parity.
- Guard time insertion.
- Receive timeout detection.
- Line Break generation.
- Programmable Baud rate generator.

DUSART

- Two synchronous/asynchronous double-buffered serial ports.
- Programmable Baud rate generator.
- Guard time insertion.
- Receive timeout detection.
- Configurable data and clock polarity.
- Data transfers msb or lsb first.

Asynchronous Interface:

- 5, 6, 7 or 8 data bits.
- 1, 1.5 or 2 stop bits.
- Even, odd or no parity.
- Line Break generation.

Synchronous Interface:

- Internal or external transmit and receive clocks.
- Full or half duplex.
- Data transfers from 1 to 16 bits with larger frames possible.
- Support for NRZ, RZ.
- Support for PM, PWM and ASK modulation using PWM timer.

I²C:

- Two wire I²C compatible port.
- Address matching.
- ACK bit and wait state insertion.
- Multi-master arbitration.
- Supports 7-bit and 10-bit addressing.

SPI:

- Master and slave operation.
- Slave chip select line.
- Programmable clock polarity and phase.

Smart Card Interface Controller:

- ISO 7816 compatible smart card interface controller.
- Received parity error detection.
- Automatic retransmission on error.
- Automatic sequencing of smart card power, reset and clock signals.
- Clock generation using PWM1 timer.

Infra-Red Link:

- Programmable baud rates.
- Support for low rate (<115.2 kbps) IrDA framing and modulation.
- Compatible with common ASK, PM, PPM (e.g. RC-5) modulation schemes.
- Half duplex operation.
- Programmable start, stop, data length, frame length and polarities.
- Programmable start/stop sequences.
- Modulation frequency generation using PWM2 timer.

User Serial Port (USR):

- Provides direct access to internal registers of each USART.
- Allows emulation of custom serial protocols.
- Up to 255 symbols per frame.
- Automatic parity generation and checking.
- Start bit edge detection.
- Tx/Rx interrupts.

Timers

- 16-bit timer TMR.
- Two 16-bit timer/counters CNT1/2.
- Two 16-bit timers PWM1/2.
- 16-bit event capture timer CAP with up to six capture inputs.
- 16-bit watchdog timer WDOG.
- 24-bit long interval timer LTMR.

External Ports

- Two 4-bit and ten 8-bit ports.
- Each port may be used for a range of peripheral functions.
- 2mA, 4mA and 8mA output current.

General Purpose I/O (GPIO)

- Up to 29 GPIO port pins.
- Individually configurable as inputs, outputs, or bidirectional.
- Outputs driven, open-drain, or tristate.

External Interrupts

- Interrupts available on all GPIO inputs.
- Level or edge sensitive interrupts.

Parallel Interface (PIO)

- Two 8/16-bit parallel ports, configurable as inputs, outputs or bidirectional.
- Outputs driven, open drain, or tristate.

12-bit ADC

- 12-bit sigma-delta ADC.
- 8kHz sample rate.
- Four channel analogue multiplexer with multiple input configurations.
- Single ended or differential inputs.
- Continuous conversion.
- On-chip temperature sensor.
- On-chip power supply monitor.

Clocks

- Uses one or two quartz crystals, a low cost 32 kHz watch crystal and/or a higher frequency 5 to 10 MHz crystal (8 MHz nominal).
- Two independent PLL multipliers.
- 5MHz crystal oscillator generates 25MHz CPU clock with low jitter.
- Low cost 32kHz watch crystal can also generate 25MHz CPU clock.
- Internal peripheral clock frequencies up to 12.5MHz.
- Selection of clock source and PLL frequency under software control.

C Compiler suite

- ANSI C Compiler.
- Validated to ANSI/ISO/FIPS-160.
- ANSI Standard Library.
- Macro Assembler.
- Software Simulator and debugger.

eICE Debug Interface

- Real-time debug port.
- Non-intrusive (real time) access to memory and CPU registers.
- Accesses to memory anywhere in CPU logical code and data spaces.
- Run, Step, Stop commands to control program execution.
- Address error detection.
- Hardware address breakpoint register.
- Flash programming.

Power Saving Features

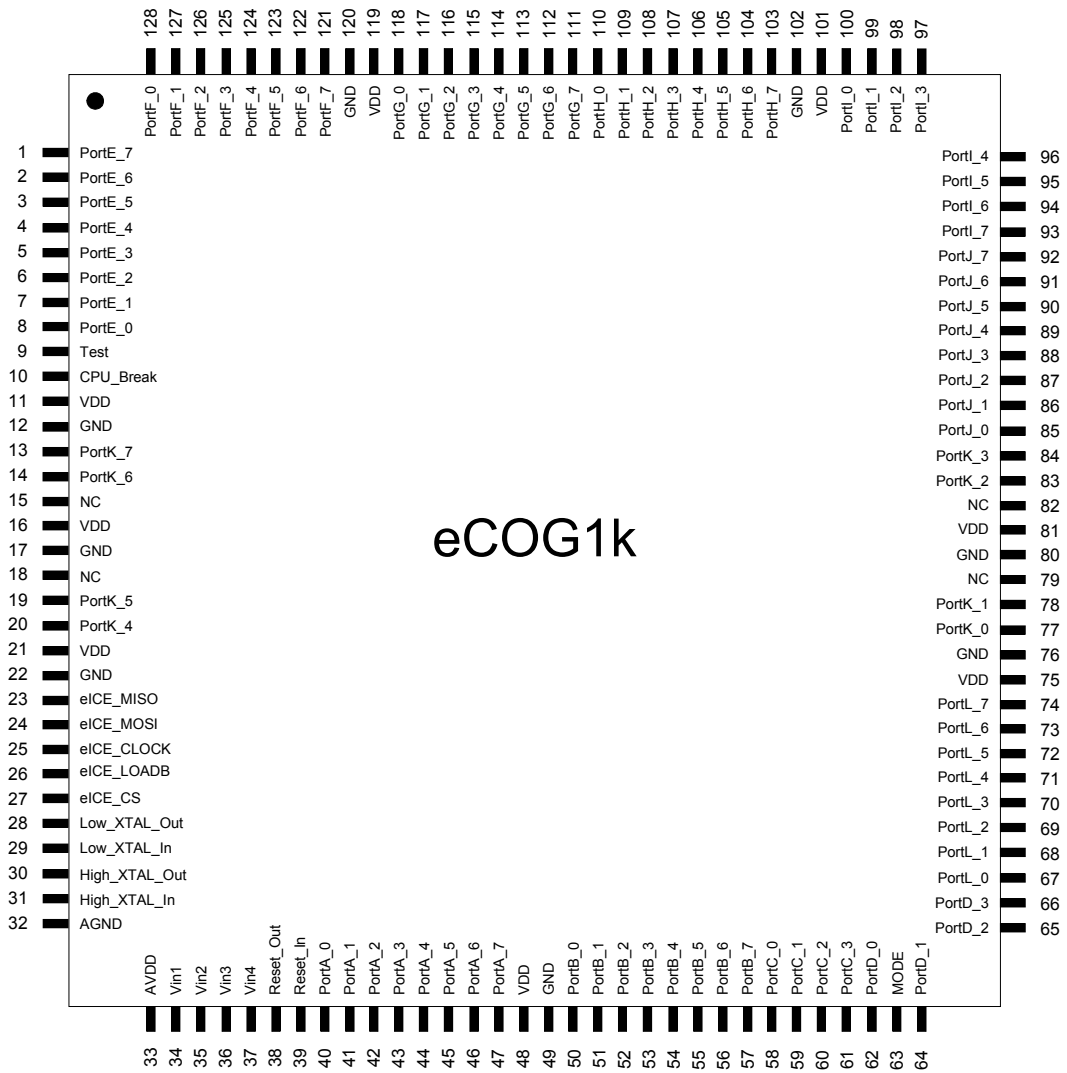
- Highly flexible peripheral clock setup.
- Sleep mode with wake on interrupts.
- All peripherals can be stopped when not in use.

Power Supplies

- Single 3.3V supply.
- On-chip power-on reset circuit.

eCOG1kG

Pin Diagram: 128 pin LQFP – K package (top view).



Pin List

Pin	Description	Pin	Description	Pin	Description	Pin	Description
1	PortE_7	33	AVDD	65	PortD_2	97	PortI_3
2	PortE_6	34	Vin1	66	PortD_3	98	PortI_2
3	PortE_5	35	Vin2	67	PortL_0	99	PortI_1
4	PortE_4	36	Vin3	68	PortL_1	100	PortI_0
5	PortE_3	37	Vin4	69	PortL_2	101	VDD
6	PortE_2	38	Reset_Out ⁶	70	PortL_3	102	GND
7	PortE_1	39	Reset_In ⁶	71	PortL_4	103	PortH_7
8	PortE_0	40	PortA_0	72	PortL_5	104	PortH_6
9	Test ¹	41	PortA_1	73	PortL_6	105	PortH_5
10	CPU_Break ¹	42	PortA_2	74	PortL_7	106	PortH_4
11	VDD	43	PortA_3	75	VDD	107	PortH_3
12	GND	44	PortA_4	76	GND	108	PortH_2
13	PortK_7	45	PortA_5	77	PortK_0	109	PortH_1
14	PortK_6	46	PortA_6	78	PortK_1	110	PortH_0

Pin	Description	Pin	Description	Pin	Description	Pin	Description
15	NC (no connect) ⁷	47	PortA_7	79	NC ⁷	111	PortG_7
16	VDD	48	VDD	80	GND	112	PortG_6
17	GND	49	GND	81	VDD	113	PortG_5
18	NC ⁷	50	PortB_0	82	NC ⁷	114	PortG_4
19	PortK_5	51	PortB_1	83	PortK_2	115	PortG_3
20	PortK_4	52	PortB_2	84	PortK_3	116	PortG_2
21	VDD	53	PortB_3	85	PortJ_0	117	PortG_1
22	GND	54	PortB_4	86	PortJ_1	118	PortG_0
23	eICE_MISO	55	PortB_5	87	PortJ_2	119	VDD
24	eICE_MOSI	56	PortB_6	88	PortJ_3	120	GND
25	eICE_CLOCK	57	PortB_7	89	PortJ_4	121	PortF_7
26	eICE_LOADB ³	58	PortC_0	90	PortJ_5	122	PortF_6
27	eICE_CS	59	PortC_1	91	PortJ_6	123	PortF_5
28	Low_XTAL_Out ⁴	60	PortC_2	92	PortJ_7	124	PortF_4
29	Low_XTAL_In ⁴	61	PortC_3	93	PortI_7	125	PortF_3
30	High_XTAL_Out ⁵	62	PortD_0	94	PortI_6	126	PortF_2
31	High_XTAL_In ⁵	63	MODE ²	95	PortI_5	127	PortF_1
32	AGND	64	PortD_1	96	PortI_4	128	PortF_0

1. The TEST and CPU_Break pins are not used in normal applications and should be connected to GND, either directly or via pull-down resistors.
2. The MODE pin is connected to VDD for the eCOG1k and to GND for the eCOG1i.
It is possible to fit an eCOG1i device in hardware designed for the eCOG1k with certain restrictions; please refer to Technical Note TN001 for more details.
3. The eICE_LOADB pin must be connected to VDD via a 4.7kΩ pull-up resistor for normal operation when the eICE debug port is not in use or disconnected. If the system is used with an external eICE programming adaptor, then the external adaptor has the 4.7kΩ pull-up resistor fitted, and the target system only needs a 100kΩ pull-up resistor connected to this signal.
It is also recommended that the remaining eICE signals are connected to GND via 100kΩ pull-down resistors as a precaution against noise.
4. If an external clock source is used instead of the 32.768 kHz quartz crystal oscillator, then the Low_XTAL_Out pin is not connected and the external clock signal is connected to Low_XTAL_In.
If the low speed clock is not required, then Low_XTAL_Out is not connected and Low_XTAL_In is connected to VDD via a 10kΩ pull-up resistor.
5. If an external clock source is used instead of the 5 MHz quartz crystal oscillator, then the High_XTAL_Out pin is not connected and the external clock signal is connected to High_XTAL_In.
If the high speed clock is not required, then High_XTAL_Out is not connected and High_XTAL_In is connected to VDD via a 10kΩ pull-up resistor.
6. The Reset_Out and Reset_In pins are not connected internally. This allows the use of an external reset circuit if required. A power-on reset signal must be connected to Reset_In for correct operation of the device, either from the internal reset circuit or from an external power-on reset circuit. To use the internal power-on reset circuit, connect Reset_Out to Reset_In, either directly or (as on the eCOG1k development boards) via external logic for any additional external reset source such as a pushbutton switch. Reset_In has a Schmitt trigger input circuit.
7. NC indicates a No Connect, these pins should not be connected in circuit.

Notes

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I²C and the I2C interface are patented by Philips Semiconductor in certain territories. Philips may demand a royalty or licence fee from designs using the I2C interface.

Declaration of RoHS Compliance

Cyan Technology Ltd hereby declares that the eCOG1kG is in full compliance with the European Directive 2002/95/EC, The Restriction of Hazardous Substances in Electrical and Electronic Equipment (RoHS).

This declaration is made based on data provided by our material suppliers, and independent analysis of all homogenous materials used in the manufacture of the product.

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