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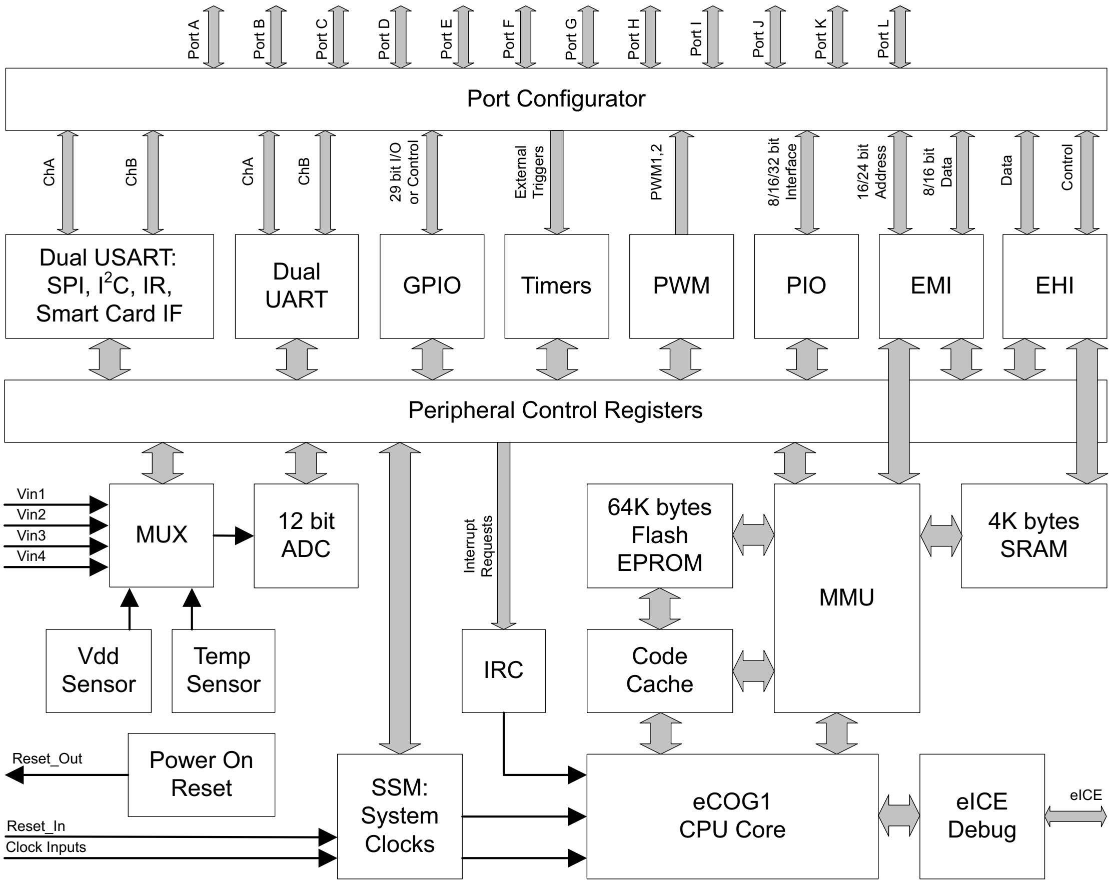
ESSENTIAL TEAMWORK FOR WINNING DESIGNS

eCOG1kG Microcontroller V5.9

The **eCOG1kG** is a low-power microcontroller, based on a 16-bit Harvard architecture, with a 24-bit linear code address space (32Mbyte) and 16-bit linear data address space (128Kbytes). The device is highly configurable, and is available in a 128 pin LQFP package. Comprehensive Development and Evaluation Kits are available. All are fully supported by Cyan's free, class-leading, integrated development environment, **CyanIDE**, which includes automatic peripheral configuration and an unrestricted ANSI C Compiler.
The eCOG1kG is a fully RoHS compliant replacement for the eCOG1k.

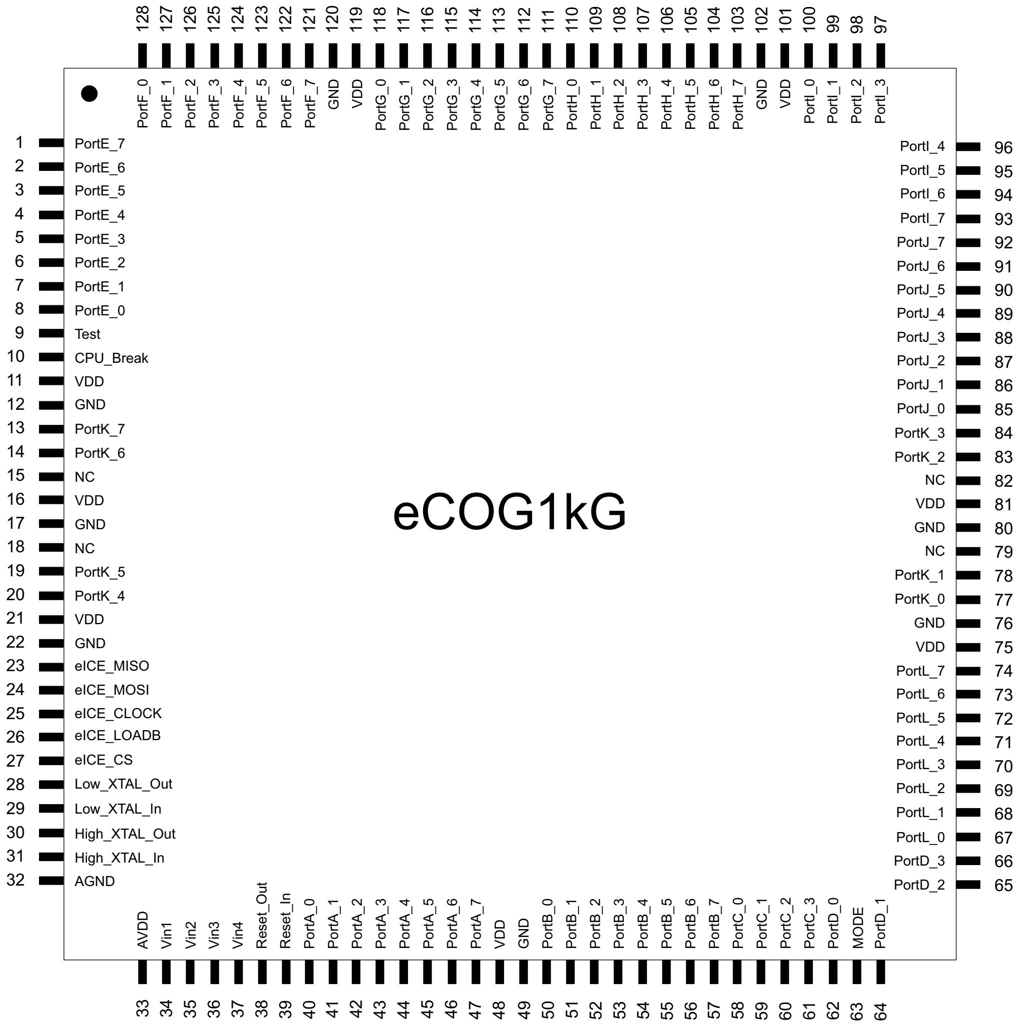
- 0 to 25MHz CPU core
- Single 3.3V supply
- Powerful arithmetic operations
- Barrel Shifter
- Harvard Architecture
- Built in Emulator (eICE)
- Low power operation
- 64Kbytes Flash
- 4Kbytes SRAM
- Memory Management Unit
- Power-saving code cache
- Code security feature
- External Host Interface
- External Memory Interface
- Fast Vectored Interrupts
- Dual UART
- Dual USART
  - SPI
  - I2C
  - Smart Card Interface
  - Infra-Red link support
- 4 channel 12-bit ADC
- Temperature Sensor
- Supply Voltage Sensor
- Power-On Reset
- 5 Multi Purpose Timers
  - Clock timer
  - 2 x counter / timer
  - 2 x PWM timer
- Capture timer with 6 inputs
- Watchdog Timer
- Long Interval Timer
- 88 digital I/O pins
- Up to 29 GPIO pins
- Parallel I/O ports
- 25MHz from watch crystal

eCOG1kG block diagram



Pin Diagram

The eCOG1kG is available in a 128 pin TQFP.
Pin pitch 0.4mm, 14x14mm body, 16x16mm at pin edge.
Top view.



Pin List

Pin No.	Description		Pin No.	Description	Pin No.	Description
1	PortE_7		44	PortA_4	87	PortJ_2
2	PortE_6		45	PortA_5	88	PortJ_3
3	PortE_5		46	PortA_6	89	PortJ_4
4	PortE_4		47	PortA_7	90	PortJ_5
5	PortE_3		48	VDD	91	PortJ_6
6	PortE_2		49	GND	92	PortJ_7
7	PortE_1		50	PortB_0	93	PortI_7
8	PortE_0		51	PortB_1	94	PortI_6
9	Test [1]	Connect to GND	52	PortB_2	95	PortI_5
10	CPU_Break [1]	Connect to GND	53	PortB_3	96	PortI_4
11	VDD		54	PortB_4	97	PortI_3
12	GND		55	PortB_5	98	PortI_2
13	PortK_7		56	PortB_6	99	PortI_1
14	PortK_6		57	PortB_7	100	PortI_0
15	NC (no connect) [7]		58	PortC_0	101	VDD
16	VDD		59	PortC_1	102	GND
17	GND		60	PortC_2	103	PortH_7
18	NC [7]		61	PortC_3	104	PortH_6
19	PortK_5		62	PortD_0	105	PortH_5
20	PortK_4		63	MODE [2]	106	PortH_4
21	VDD		64	PortD_1	107	PortH_3
22	GND		65	PortD_2	108	PortH_2
23	eICE_MISO	eICE debug port	66	PortD_3	109	PortH_1
24	eICE_MOSI		67	PortL_0	110	PortH_0
25	eICE_CLOCK		68	PortL_1	111	PortG_7
26	eICE_LOADB [3]		69	PortL_2	112	PortG_6
27	eICE_CS		70	PortL_3	113	PortG_5
28	Low_XTAL_Out [4]	32.768 kHz quartz crystal	71	PortL_4	114	PortG_4
29	Low_XTAL_In [4]		72	PortL_5	115	PortG_3
30	High_XTAL_Out [5]	5 MHz quartz crystal	73	PortL_6	116	PortG_2
31	High_XTAL_In [5]		74	PortL_7	117	PortG_1
32	AGND	Analogue GND	75	VDD	118	PortG_0
33	AVDD	Analogue V_{DD}	76	GND	119	VDD
34	Vin1	Analogue input channel 1	77	PortK_0	120	GND
35	Vin2	Analogue input channel 2	78	PortK_1	121	PortF_7
36	Vin3	Analogue input channel 3	79	NC [7]	122	PortF_6
37	Vin4	Analogue input channel 4	80	GND	123	PortF_5
38	Reset_Out [6]	Active high reset output from internal power-on reset circuit	81	VDD	124	PortF_4
39	Reset_In [6]	Active high reset input	82	NC [7]	125	PortF_3
40	PortA_0		83	PortK_2	126	PortF_2
41	PortA_1		84	PortK_3	127	PortF_1
42	PortA_2		85	PortJ_0	128	PortF_0
43	PortA_3		86	PortJ_1		

Table 1: eCOG1kG pin list

Pin Functions

Label	Function	I/O
AGND	Analogue GND	PWR
AVDD	Analogue power supply 3.3V	PWR
CPU_Break [1]	CPU Break input	I
eICE_CLOCK	eICE clock input	I
eICE_LOADB [3]	eICE Load Byte handshake signal	I/O
eICE_MISO	eICE Master In Slave Out	O
eICE_MOSI	eICE Master Out Slave In	I
GND	Digital GND	PWR
High_XTAL_In [4]	High frequency crystal oscillator input	I
High_XTAL_Out [4]	High frequency crystal oscillator output	O
Low_XTAL_In [5]	Low frequency crystal oscillator input	I
Low_XTAL_Out [5]	Low frequency crystal oscillator output	O
MODE [2]	Mode configuration pin	I
NC [7]	No Connect	
PortA_0-7	Port A pins 0-7	I/O
PortB_0-7	Port B pins 0-7	I/O
PortC_0-3	Port C pins 0-3	I/O
PortD_0-3	Port D pins 0-3	I/O
PortE_0-7	Port E pins 0-7	I/O
PortF_0-7	Port F pins 0-7	I/O
PortG_0-7	Port G pins 0-7	I/O
PortH_0-7	Port H pins 0-7	I/O
PortI_0-7	Port I pins 0-7	I/O
PortJ_0-7	Port J pins 0-7	I/O
PortK_0-7	Port K pins 0-7	I/O
PortL_0-7	Port L pins 0-7	I/O
Reset_In [6]	Power-on reset input	I
Reset_Out [6]	Power-on reset sense output	O
Test [1]	Test select input	I
VDD	Digital power supply 3.3V	PWR
Vin1-4	ADC analogue inputs	I

Table 2: eCOG1kG pin functions

1 The Test and CPU_Break pins are not used in normal applications and should be connected to GND, either directly or via pull-down resistors.

2 The MODE pin is connected to V_{DD} for the eCOG1kG and to GND for the eCOG1i.
It is possible to fit an eCOG1i device in hardware designed for the eCOG1kG with certain restrictions;
refer to Technical Note TN001 for more details.

3 The eICE_LOADB pin must be connected to V_{DD} via a pull-up resistor for normal operation when the eICE debug port is not in use or disconnected. A 4.7kΩ pull-up resistor is required when the eICE port is in use, to reduce the rise time on this open-drain signal and increase the speed of eICE data transfers. If the system is used with an external eICE programming adaptor, then the external adaptor has the 4.7kΩ pull-up resistor fitted, and the target system needs only a 100kΩ pull-up resistor connected to this signal.
It is also recommended that the eICE input signals (eICE_CLK, eICE_MOSI, eICE_CS) are connected to GND via 100kΩ pull-down resistors as a precaution against noise when the eICE port is not in use or disconnected.

4 If an external clock source is used instead of the 5 MHz quartz crystal oscillator, then the High_XTAL_Out pin is not connected and the external clock signal is connected to High_XTAL_In through a 100pF series coupling capacitor.
If the high speed clock is not required, then High_XTAL_Out is not connected and High_XTAL_In is connected to V_{DD} via a 10kΩ pull-up resistor.

5 If an external clock source is used instead of the 32.768 kHz quartz crystal oscillator, then the Low_XTAL_Out pin is not connected and the external clock signal is connected directly to Low_XTAL_In. No coupling capacitor is required.
If the low speed clock is not required, then Low_XTAL_Out is not connected and Low_XTAL_In is connected to V_{DD} via a 10kΩ pull-up resistor.

6 The Reset_Out and Reset_In pins are not connected internally. This allows the use of an external reset circuit if required. An active high power-on reset signal must be connected to Reset_In for correct operation of the device, either from the internal reset circuit or from an external power-on reset circuit. To use the internal power-on reset circuit, connect Reset_Out to Reset_In, either directly or via external logic for any additional external reset source such as a pushbutton switch.
The Reset_In input has a Schmitt trigger input circuit.

7 NC indicates a No Connect, these pins should not be connected in circuit.

Description

This section gives a brief description of the main features of the eCOG1kG device. The eCOG1kG is a fully RoHS compliant replacement for the eCOG1k and is functionally identical. Any reference to the eCOG1k in user documentation is applicable to the eCOG1kG.

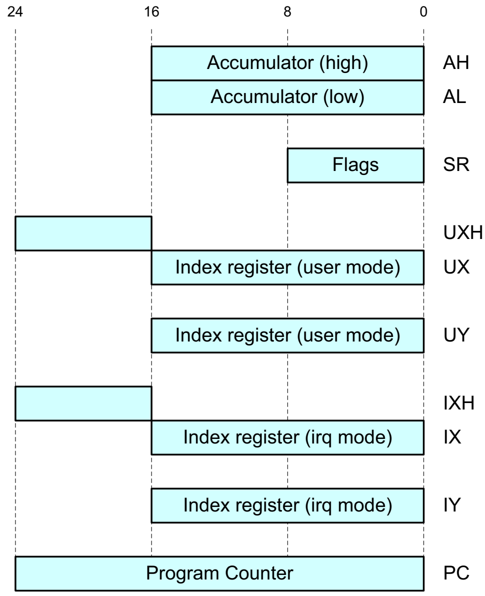
For a complete description, see the eCOG1k User Manual.

CPU

The eCOG1k has an advanced high speed, low power CPU with an instruction set targeted at high level languages, in particular C. The CPU operates at internal clock frequencies up to 25MHz. Full details of the instruction set are contained in the eCOG1 Macro Assembler User Manual.

The main features of the processor are:

- 16-bit RISC.
- Sleep mode to support low power applications.
- Harvard architecture (separate internal address and data buses for faster memory accesses).
- 16-bit data space addressing range (64K by 16 bits).
- 24-bit code space addressing range (16M by 16 bits).
- Support for debugging and multiple breakpoints.
- Single level of interrupt.
- Powerful mathematical functions including:
  - 16 by 16 signed and unsigned multiply.
  - 32 by 16 unsigned divide.
  - Single cycle barrel shifter.



Instruction Set

The eCOG1 instruction set includes 42 instructions with 6 addressing modes. Most instructions operate on 16-bit word data values, while the LD and ST instructions also have variants for handling byte data values.

Address mode	Syntax	Data address
Immediate	#arg	arg
Direct	@arg	Contents of address (arg)
Indexed X	@(arg,x)	Contents of address (arg + X reg)
Indexed Y	@(arg,y)	Contents of address (arg + Y reg)

Table 3: Data addressing modes

Address mode	Syntax	Branch address (new PC value)
PC relative	arg	PC + arg
X relative	arg,x	XH:X + arg
Direct	@arg	XH:contents of address (arg)
Indexed Y	@(arg,y)	XH:contents of address (arg + Y reg)

Table 4: Branch addressing modes

Operating Modes

There are three independent aspects of the processor operating modes.

Processor State	awake or asleep
Processor Mode	interrupt or user mode
Program State	running or stopped (used when debugging)

Processor State

When the processor is awake, it fetches and executes instructions normally. When the processor is asleep, no instructions are executed. The *SLEEP* instruction changes from the awake to the asleep state, and selected peripherals are stopped automatically to reduce power consumption. External I/O activity triggers a wake up event, and selected peripherals are started automatically.

Processor Mode

Interrupts from internal or external peripherals are enabled in user mode. When an interrupt is serviced, the processor changes from user to interrupt mode. No further interrupts are serviced until the processor completes the current interrupt service routine and returns with an *RTI* instruction.

In user mode, the processor uses the UX and UY registers. In interrupt mode, it uses the IX and IY registers. It is possible to switch between user and interrupt modes in software by changing the state of the interrupt mode bit in the flags register.

Program State

When executing an application, the program is in the normal running state. When debug mode is enabled via the eICE debug port, the program can change to the stopped state on the following events.

- A *BRK* instruction is executed.
- The PC register becomes equal to one of the code address breakpoint registers.
- A data space access matches the configuration in the data breakpoint registers.
- An eICE *stop* command is received via the debug port.

Once the program is stopped, a *run* command received via the eICE debug port restarts execution.

Instruction Cache

The eCOG1k has an on-chip instruction cache, implemented using fast SRAM. It is arranged as two banks of 1K bytes (512 words) of memory. This fast memory area can be configured as a single 512 word cache, a two way set associative 256 word cache, 1K words of static RAM, or a combination of 256 words of RAM and a single 256 word cache.

The cache increases the processing speed when executing code from flash memory, and reduces the power consumption. The instruction cache also provides support for large numbers of breakpoints when debugging. Many *BRK* instructions can be locked in the cache as soft breakpoints, even when executing code from internal flash memory.

Memory Management Unit

The Memory Management Unit (MMU) allows a variety of internal and external memories to be combined into a single logical memory structure. The memory structure or model has both code space and data space address locations to match the Harvard architecture CPU. The MMU provides both code space translations for program code and data space translations for variables and constants. A single physical memory can be mapped into both code and data space.

Flash Memory

The eCOG1k contains up to 64K bytes of on-chip flash memory for program and data storage, organised as 32K x 16 bit words. The flash memory is programmed with and operates from the eCOG1k's normal 3.3V supply; no external high voltages are required for erasing or programming.

In addition to the main program/data area in flash memory, there is an additional block of 64 x 16-bit words, used as an information block area. These locations are not accessible by direct memory read/ writes, but are accessed indirectly via peripheral registers.

The lower four words in the information block are used for read and write protection of the main flash memory sectors and the information block itself. The remaining words in the information block may be used to hold user data, such as application configuration data, product serial numbers, version numbers, etc.

The flash memory main block contains 8 sectors of 4K words, with each sector arranged as 16 pages of 256 words. The information block is one sector of 64 words, arranged as 2 pages of 32 words. The following table shows the sector addresses in the flash memory main block:

Sector	**A14**	**A13**	**A12**	**Sector size (Kwords)**	**Address Range (hexadecimal)**
SA0	0	0	0	4	0x0000-0x0FFF
SA1	0	0	1	4	0x1000-0x1FFF
SA2	0	1	0	4	0x2000-0x2FFF
SA3	0	1	1	4	0x3000-0x3FFF
SA4	1	0	0	4	0x4000-0x4FFF
SA5	1	0	1	4	0x5000-0x5FFF
SA6	1	1	0	4	0x6000-0x6FFF
SA7	1	1	1	4	0x7000-0x7FFF

Table 5: Flash memory organisation

The flash memory can be programmed via the eICE debug port or in-system by the CPU. It supports the following functions.

- Read accesses in code space or data space.
- Information block reads via peripheral registers.
- Complete flash memory erase (chip erase).
- Page erase.
- Programming of single words.
- Buffered programming of up to 32 words in a single page in one write operation.
- Individual sector write and read protection.

Internal Memory

The eCOG1k contains 4K bytes of on-chip static RAM, organised as 2K x 16 bits. It can be used as data or code memory. If the instruction cache is disabled, it can be used as an additional 2K bytes of SRAM (1K x 16 bits) if required.

Interrupts

After power on or a hardware reset, execution starts from code space address zero mapped into the internal flash memory. The first four words of code space should contain an instruction to branch to the start of the application code.

The eCOG1k CPU supports 64 vectored interrupts and exceptions. The interrupt vector table follows immediately after the four words containing the reset vector branch instruction. Each vector contains a 16-bit offset. When an interrupt occurs, the interrupt service routine address is found by reading the corresponding 16-bit vector offset and sign-extending it to a 24-bit code space address. It follows that all interrupt service routines must be located in the first 32K words (address range 0x000000 to 0x007FFF) or last 32K words (address range 0xFF8000 to 0xFFFFFF) of code space.

Interrupt	Vector	**Description**
reset	0x00 0x01 0x02 0x03	Reset vector at location 0x0. User must insert a branch instruction at this address.
_ex_debug	0x04	Debug exception
_ex_wdog_exp	0x05	Timer/counters, watchdog timer expired
_ex_adr_err	0x06	MMU: access to an unmapped address EMI: access to a chip select that is disabled
reserved	0x07	
_ex_tim	0x08	Exception interrupt from timer/counter module
reserved	0x09	
_ex_usarta	0x0A	Exception interrupt from DUSART channel A
_ex_usartb	0x0B	Exception interrupt from DUSART channel B
_ex_uarta	0x0C	Exception interrupt from DUART channel A
_ex_uartb	0x0D	Exception interrupt from DUART channel B
_int_tmr_exp	0x0E	Timer/counters, timer TMR underflow
_int_cnt1_exp	0x0F	Timer/counters, counter CNT1 underflow
_int_cnt2_exp	0x10	Timer/counters, counter CNT2 underflow
_int_cnt1_match	0x11	Timer/counters, counter CNT1 comparator match
_int_cnt2_match	0x12	Timer/counters, counter CNT2 comparator match
_int_pwm1_exp	0x13	Timer/counters, PWM1 underflow
_int_pwm2_exp	0x14	Timer/counters, PWM2 underflow
_int_pwm1_match	0x15	Timer/counters, PWM1 transition value match
_int_pwm2_match	0x16	Timer/counters, PWM2 transition value match
_int_cap_exp	0x17	Timer/counters, input capture timer overflow
_int_cap1	0x18	Timer/counters, input capture timer event 1
_int_cap2	0x19	Timer/counters, input capture timer event 2
_int_cap3	0x1A	Timer/counters, input capture timer event 3
_int_cap4	0x1B	Timer/counters, input capture timer event 4
_int_cap5	0x1C	Timer/counters, input capture timer event 5
_int_cap6	0x1D	Timer/counters, input capture timer event 6
_int_ltmr_exp	0x1E	Timer/counters, long interval timer LTMR underflow
reserved	0x1F	
reserved	0x20	
reserved	0x21	
reserved	0x22	
reserved	0x23	
reserved	0x24	
reserved	0x25	
reserved	0x26	
_int_usarta_rx_rdy	0x27	DUSART channel A receive port ready
_int_usarta_tx_rdy	0x28	DUSART channel A transmit port ready
_int_usartb_rx_rdy	0x29	DUSART channel B receive port ready

Table 6: Interrupt and exception vectors

Interrupt	Vector	**Description**
_int_usartb_tx_rdy	0x2A	DUSART channel B transmit port ready
_int_sci_tx_done	0x2B	DUSART smart card transmit data complete
_int_sci_tx_err	0x2C	DUSART smart card transmit error detected
_int_sci	0x2D	DUSART general smart card interrupt
_int_ifr_tx_done	0x2E	DUSART infrared transmit data complete
_int_ifr_rx_done	0x2F	DUSART infrared receive data complete
_int_ifr_rx_err	0x30	DUSART infrared receive error detected
_int_ifr_frame_done	0x31	DUSART infrared frame complete
_int_uarta_tx_rdy	0x32	DUART A transmit port ready
_int_uarta_rx_rdy	0x33	DUART A receive port ready
_int_uartb_tx_rdy	0x34	DUART B transmit port ready
_int_uartb_rx_rdy	0x35	DUART B receive port ready
_int_ehi	0x36	EHI module interrupt
_int_gpio	0x37	GPIO interrupt (edge or level detect)
_int_adc	0x38	ADC data ready interrupt (conversion complete)
reserved	0x39	
reserved	0x3A	
reserved	0x3B	
reserved	0x3C	
reserved	0x3D	
reserved	0x3E	
reserved	0x3F	

Table 6: Interrupt and exception vectors

eICE Debug Interface

The eICE debug interface provides a serial communication interface allowing an external device (the eICE master) to have read and write access in the memory and register space of the eCOG1 (slave), and to control the CPU state and program execution with various debug commands. Access to memory and registers can take place in real time, with the CPU running or halted.

eICE functions include:

- Interactive, real time debug.
- Non-intrusive (real time) access to memory and CPU registers.
- Single or double memory accesses anywhere in CPU logical code and data spaces.
- Run/Step/Stop commands to control program execution.
- Address error detection.
- 32 bit data ICE operations.
- Synchronised (deterministic) access mode available by inserting instructions in code.
- Hardware address breakpoint register.
- Flash programming.
- Version register to identify ICE interface.

The eICE debug interface requires only a 10-pin header on the target system. A low cost USB eICE adaptor plugs into this header and connects to the host PC via USB. This adaptor is used by the CyanIDE software development tool, allowing single stepping at C source code level and inspection or modification of variables or memory, while running the application on the target system.

Peripherals

This section gives a brief description of the eCOG1k device peripherals. For a complete description, see the eCOG1k User Manual.

System Support Module

The System Support Module (SSM) controls all internal clocks and reset signals for the eCOG1k CPU and peripherals.

The SSM has four principal functional blocks.

- Clock oscillators and PLL multipliers.
- CPU/memory clock selector.
- Divider chains.
- Peripheral clock selectors.

Clock sources

Four clock sources are used to provide all eCOG1k internal system clocks. Two crystal oscillators provide accurate reference clocks, which can be driven into two PLL multipliers providing a further two reference clocks.

- Low reference oscillator.
  A low power 32kHz oscillator using an external quartz watch crystal.
- Low PLL.
  Phase locked loop multiplier, clocked by the low reference oscillator at 32kHz. It has a fixed multiplication factor of x150, giving an output frequency of 4.9152MHz.
- High reference oscillator.
  A high performance oscillator using an external 4-10MHz quartz crystal (5MHz nominal).
- High PLL.
  Phase locked loop multiplier, clocked by the high reference oscillator at 5MHz. It has a fixed multiplication factor of x20, giving an output frequency of 100MHz.

CPU/Memory Clock Selector

The CPU/memory clock selector contains logic for detecting valid running clocks and selecting the master clock from the available clock signals. It also provides a prescaler and divider to control the frequencies of the clocks to both the CPU and the memory subsystem.

Divider Chains

Four 16-bit divider chains, each clocked from one of the principal system clock sources, provide the source clock signals for all the internal peripheral modules. The divider chains provide a range of clock frequencies to the peripherals, to be selected according to the speed of the peripheral or any low power requirements of the application. The output frequency division factors range from $\div 2^2$ to $\div 2^{17}$. The smallest division factor from the high PLL clock is $\div 2^3$, giving a maximum peripheral clock frequency of 12.5MHz.

Peripheral Clock Selectors

Each of the 16 outputs from the four divider chains are fed into the peripheral clock selector block, giving a total of 64 possible clock frequencies for each peripheral from the four clock sources. For each peripheral module, one output from one of the four divider chains is selected to provide its clock signal.

Summary

The source clock and peripheral clock selections provide an extremely flexible system for controlling independently the frequencies of the clock signals to each peripheral. This has significant benefits in managing the power consumption of the device. High frequency clocks can be provided selectively to the high speed peripherals that need them, while low speed peripherals can use low frequency clocks, reducing unnecessary power consumption. Unused peripherals can have their clock stopped altogether, reducing their supply current to a minimum.

The following diagram shows the complete eCOG1k SSM clocking scheme.

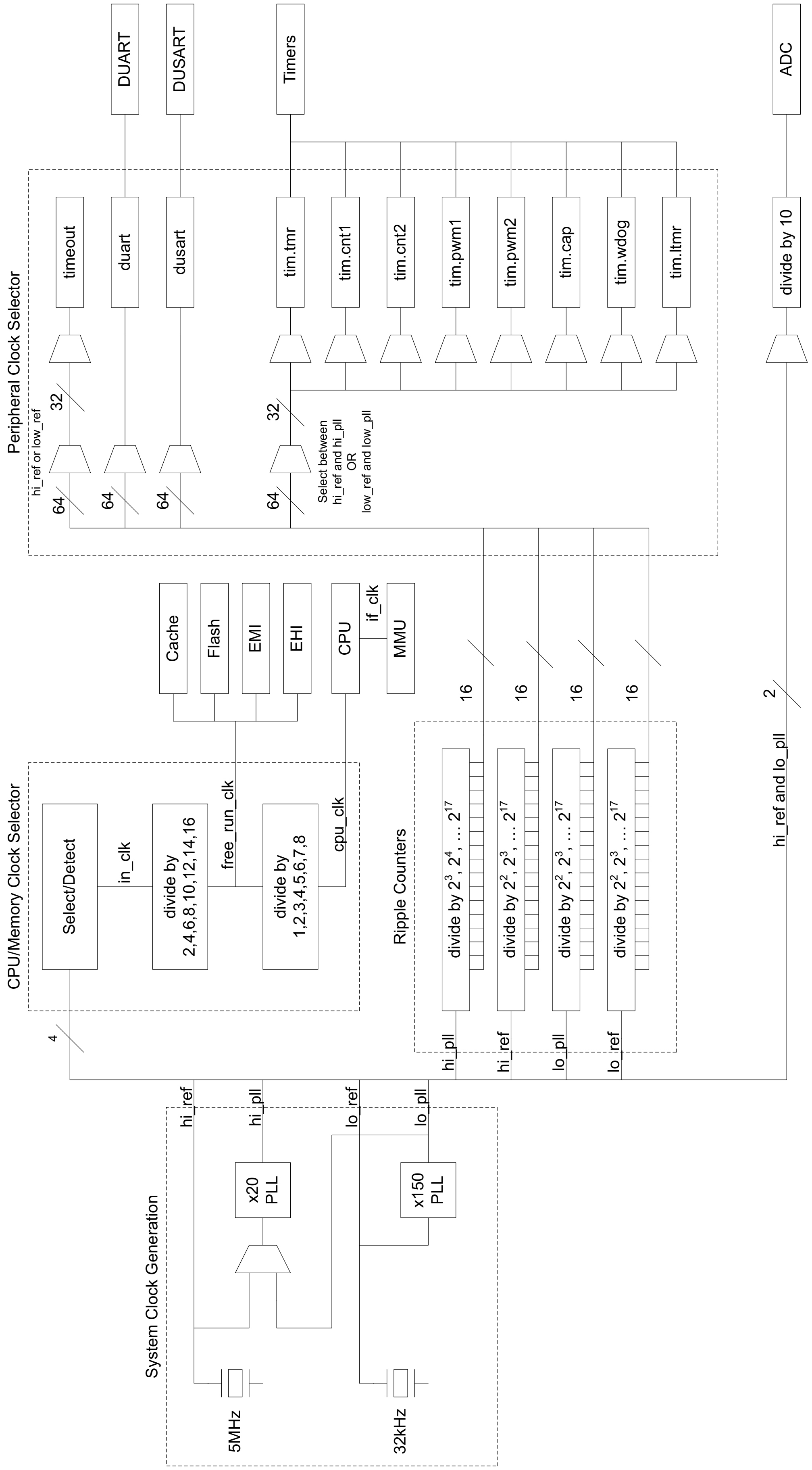


Figure 1: Detailed eCOG1k clocking scheme

Port Configurator

The eCOG1k device includes twelve I/O ports, consisting of ten 8-bit ports and two 4-bit ports. The Port Configurator selects how the internal peripherals are connected to the external I/O ports. Each port may be assigned to a specified peripheral function, used for general-purpose I/O, or disabled.

The port configuration options are described in more detail later in this data sheet and in the eCOG1k User Manual.

General-Purpose I/O

As part of the peripheral selections available through the Port Configurator, I/O port pins can be configured for general-purpose I/O (GPIO) if required. GPIO pins can be configured as inputs, outputs or bidirectional. All GPIO pins can be configured for interrupts, either edge-triggered or level-triggered.

- Up to 29 GPIO port pins.
- Individually configurable as inputs, outputs or bidirectional.
- Outputs driven, open-drain or tristate controlled.
- 2mA source/sink output current (ports A, B, C, D, J).
- 4mA source/sink output current (ports E, F, G, H, I, L).
- 8mA source/sink output current (port K).

Parallel I/O

eCOG1k also contains parallel I/O (PIO) peripheral functions. PIO allows users to control groups of 8 or 16 I/O signals at a time, whereas the GPIO function provides users with signals that can be individually controlled.

PIO is typically used for bus signals where it is necessary for the whole bus to change simultaneously, for example driving parallel output data signals into a DAC. GPIO is typically used for controlling individual signals, for example the output update signal to a DAC or start conversion signal to an ADC.

- Two 8/16-bit parallel data ports, configurable as inputs, outputs or bidirectional.
- Outputs driven, open-drain or tristate controlled.

Timers and Counters

The timer/counter (TIM) peripheral module provides a set of hardware timing and counting functions. Eight independent timers support a range of functions.

- 16-bit timer TMR.
- Two 16-bit timer/counters CNT1, CNT2.
- Two 16-bit timers PWM1, PWM2, providing a pulse-width modulated output signal.
- 16-bit watchdog timer WDOG.
- 16-bit event capture timer CAP with up to 6 capture inputs.
- 24-bit long interval timer LTMR.

Timer

The clock timer TMR is a 16-bit down count timer. An interrupt is generated when the timer counts past zero. The count duration may be preset or reset at any time. When enabled, the timer counts at its input clock frequency, set by the SSM.

Counter

The two timer/counters CNT1 and CNT2 are 16-bit down counters. An interrupt is triggered when the counter passes the value stored in a compare register. A second interrupt is generated when the counter passes zero. The count duration may be preset or reset at any time, and reload can be manual or automatic. In addition these timers may be configured to count on either or both edges of an external clock input.

When configured as timers, they count at their input clock frequencies, set by the SSM. Alternatively, when configured as counters, they count when a selected edge occurs on their external clock signal inputs. These timer/counters are therefore suitable for counting external events in a target system.

PWM

The two PWM timers are implemented as 16-bit down counters. An interrupt is generated when the timer passes a ‘transition’ value stored in one of the configuration registers, and a second interrupt is generated when the timer passes zero. The count duration may be preset or reset at any time.

When enabled, the PWM timers count at their input clock frequencies, set by the SSM. The PWM output signal inverts on each interrupt (transition or zero value). The sense of the output signal is programmable.

Typical applications are to generate a variable frequency output or a pulse width modulated output. Note that by adding an external low-pass filter, it is possible to use a PWM output as a low speed digital-to-analogue converter (DAC).

Capture Timer

The input capture timer CAP is a 16-bit up counter. An interrupt is generated when the timer wraps around to zero, and it may be reset to zero at any time. When enabled, the capture timer counts at its input clock rate, set by the SSM.

The capture timer value is transferred to one of the six capture registers when an edge is detected on one of the six capture inputs. Capture inputs 1-4 store all 16 bits of the capture timer value, while capture inputs 5 and 6 store only the high 8 bits of the capture timer value.

Watchdog Timer

The watchdog timer WDOG is a 16-bit down counter. The count duration may be preset to a new value or reset to the current period value at any time. When enabled, the watchdog timer counts at its input clock frequency, set by the SSM.

When the watchdog timer reaches zero, a watchdog timeout exception interrupt is generated and the counter restarts automatically to begin a new countdown period. In addition, it also forces the CPU clock active at its slowest rate. This is to enable recovery from the situation where the incorrect number of wait states have been set for code space memory. User software must therefore reconfigure the device clocks after this interrupt occurs.

Long Interval Timer

The long interval timer LTMR is a 24-bit down counter, allowing a maximum count of 2^{24}. An interrupt is generated when the timer passes zero. The upper 16 bits of the timer may be set at any time to the value in a load register; the lower 8 bits are reset to zero when the upper 16 bits are written. When enabled, the long interval timer counts at its input clock frequency, set by the SSM.

DUART

The eCOG1k includes a DUART module, providing two separate UART channels, labelled A and B.

The two UART channels support the following features:

- Programmable format: 5, 6, 7 or 8 data bits; 1, 1.5 or 2 stop bits; even, odd or no parity.
- Programmable baud rate divider.
- 8-bit and 16-bit transmit data registers (one and two data frames).
  Interrupts generated on transmit ready and overflow.
- 8-bit and 16-bit receive data registers (one and two data frames).
  Receive data ready interrupt generated on one or two bytes received.
- Oversampled received data with noise filter.
  Receiver error detection for false start bits, parity and frame errors.
- Configurable data signal polarities.
- Receive timeout detection of 1 to 63 bit periods.
- Line Break (15 consecutive data zero bits) generation in software, detection in hardware.
- Power saving features to start the UART clock automatically when the receiver detects a start bit and to hold the clock active during transmission.
- Operates independently of the CPU, allowing the CPU to be put to sleep while the DUART transmit or receive is still active.

DUSART

The DUSART is a general purpose dual synchronous/asynchronous serial port. Each of the two channels can implement one of the supported protocols. Note that each serial protocol may only be used once, the same protocol cannot be used simultaneously on both channels (except for the generic User Serial Port function which can be used on both channels).

The following protocols are supported by the DUSART peripheral.

- Standard UART.
- Serial Peripheral Interface (SPI).
- I^{2}C multi-master, multi-drop 2 wire bus.
- Low rate IrDA and general purpose infrared controller protocol (IFR).
- ISO 7816 smart card interface (SCI).
- Generic User Serial Port (USR).

UART

The UART implementation within the DUSART peripheral provides all of the common functions required.

- Programmable format: 5, 6, 7 or 8 data bits; 1, 1.5 or 2 stop bits, even, odd or no parity.
- Programmable baud rate.
- 8-bit and 16-bit transmit data registers (one and two data frames).
  Interrupts generated on transmit ready and overflow.
- 8-bit and 16-bit receive data register (one and two data frames).
  Interrupts generated on one or two bytes received.
- Configurable data signal polarities.
- Transmit break control.
- Receive break interrupt and status bit.
- Receive frame error detection interrupt and status bit.
- Receive timeout.
- Transmit guard time.

SPI

SPI is one of the protocols supported by the DUSART peripheral. This gives the eCOG1k both SPI master and slave capability, with the option of supporting multiple slave devices in master mode.

The SPI function includes the following features.

- Master and slave operation.
- Programmable serial clock polarity and phase.
- Data transfer size 1 to 16 bits.
- Programmable serial clock frequency (master mode).
- Slave chip select, an output in master mode and an input in slave mode.

I^{2}C

The Inter-IC Communication standard (I^{2}C) is a bidirectional, multi-drop, multi-master, two wire interface for connecting microcontrollers to their peripheral devices such as memories and interface ICs. It is capable of serial data transfer up to speeds of 100 kbps (standard), 400 kbps (fast mode) and 3.4 Mbits/s (high speed mode). The DUSART I^{2}C function supports 100 kbps operation only.

The I^{2}C function includes the following features.

- Start, stop, and restart operations.
- Address matching and arbitration.
- Supports multi-master and master/slave operations.
- Automatic acknowledge generation.
- 7 bit, 10 bit and broadcast addressing.

IFR

The IFR function in the DUSART provides a configurable CODEC designed for the transmission and reception of infra-red data frames. Input signals should be demodulated externally before being supplied to the device for decoding. The IFR transmit data output signal may be provided both modulated and unmodulated.

The module is designed to be flexible, supporting current consumer protocols (RC-5, ASK, PPM) and other infra-red protocols. Some support is also provided for low-rate IrDA format signals.

SCI

The Smart Card Interface (SCI) function in the DUSART contains all of the logic functionality required for the terminal (controller) part of a smart card interface. Activation and deactivation sequences are supported with various degrees of (configurable) automation. Protocol type T=0 is supported; refer to the Smart Card standard ISO 7816 parts 1-10.

The SPI function includes the following features.

- Card activation sequencer with hardware delay timer.
- Card deactivation sequencer with hardware delay timer.
- Data transmit sequencer with hardware guard time, error detection and retransmission.
- Data receive sequencer with hardware error detection and retransmit request.
- Programmable signal polarities.
- UART serial port operation.
- Normal or inverse data convention.

USR

The USR function provides flexible, low-level access to the core features of the DUSART peripheral. It may be used to implement synchronous or asynchronous protocols that are not already supported by the other DUSART functions, for example a 9-bit UART protocol, with less software overhead than a GPIO based emulation.

The USR function includes the following features.

- Provides direct access to internal USART features.
- Allows custom serial protocols to be emulated.
- Up to 255 symbols per frame.
- Automatic parity generation and checking.
- Start bit edge detection.
- Transmit and receive data interrupts.

External Memory Interface

The External Memory Interface (EMI) allows connection of external memories to both code and data space of the CPU via the memory manager.

The EMI supports two memory interface modes:

- Bus Interface Mode:
  (a) Independent 25-bit address and 8-bit data, or
  (b) Multiplexed 24-bit address and 16-bit data.
  This interface can connect to external devices such as flash memory, SRAM, ROM or memory mapped peripherals.
- SDRAM Interface Mode:
  Supports direct connection to single data rate SDRAM (up to 32Mbytes) with no external components.

The EMI has two chip select outputs that can be programmed individually to operate with either the SDRAM or Bus interfaces. If both chip selects are configured for the same interface type, then the settings are the same for both external memories. This means that the memories' timing parameters and control signals must be compatible.

The EMI peripheral includes the following features.

- 8 or 16-bit data bus.
- 16 or 24-bit address bus.
- Multiplexed address/data in 16-bit data bus mode.
- External devices can be mapped into both code and data space.
- Configurable cycle and signal timing.
- Four SDRAM row/column address multiplexing schemes.
- Supports SDRAM auto and self refresh.
- Supports low-power SDRAM suspend/standby modes.
- Single cycle data space accesses.
- Burst accesses in code space, using instruction cache.
- Add wait states for slow devices with the EMI_WAIT input signal.

External Host Interface

The External Host Interface (EHI) allows the eCOG1k and an external processor to share an area of the eCOG1k internal SRAM which can be directly accessed by both the eCOG1k processor and the external device. The eCOG1k processor can write and read to the locations via the MMU, whilst the external device can write and read to the locations via the EHI.

The external device has two modes in which it can access the internal SRAM. In MMP mode, the eCOG1k is seen as a memory mapped peripheral and the shared SRAM area is mapped into the memory map of the external device. In DMA mode, the external device accesses the shared SRAM area using the DMA control signals.

MMP mode is intended for small random accesses, whilst DMA mode is intended for large block copy data transfers. The EHI provides a means for enabling both modes to assist the interleaving of large and small data accesses.

The EHI peripheral includes the following features.

DMA mode:

- Supports master and slave mode timings.
- 16 or 32-bit data bus.
- Request and acknowledge control signals.
- Programmable transfer cycle timing in master mode.
- DMA connection into internal SRAM.
- 11-bit block address, maximum block size 256 bytes.

MMP mode:

- Selectable block size: 256 x 16-bit data, or 8 x 32-bit data.
- Three control signals: chip select, read/write direction, and wait.
- Configurable control signal senses.

Analogue Inputs

The eCOG1k includes a 12-bit sigma-delta analogue-to-digital converter which operates at a fixed sample rate. It can sample up to 4 different external analogue signals in addition to an internal supply voltage sensor and chip temperature sensor. The ADC can also be operated in differential mode to sample the difference between two external analogue signals. This can be used to remove common mode noise on a balanced signal pair.

The main features of the ADC peripheral include:

- 12-bit sigma-delta Analogue to Digital Converter (ADC).
- Internal 1.25V nominal bandgap voltage reference.
- Analogue multiplexer with two internal and four external input signals.
- Internal ADC inputs for temperature sensor and analogue supply voltage sensor.
- Single-ended and differential input configurations.
- Sample rate of 7.680 ks/s or 7.8125 ks/s at 12 bits resolution.
- Interrupt on conversion complete.

The analogue block also includes the on-chip power on reset circuit.

Port Select Options

The eCOG1k device pins are connected to 12 I/O ports labelled A to L. Different peripheral functions can be mapped to these ports to define the operation of each pin. This section contains tables listing the peripheral signals available for each of the configurable ports. For further details, refer to the eCOG1k User Manual.

Port A

port.sel1.a	**0**	**1**	**3**	**4**	**6**
A_0	SC_DATA_IN	SPI_SCLK	SPI_SCLK	SC_DATA_IN	SPI_SCLK
A_1	SC_DATA_OUT	SPI_MOSI	SPI_MOSI	SC_DATA_OUT	SPI_MOSI
A_2	SC_RST	SPI_MISO	SPI_MISO	SC_RST	SPI_MISO
A_3	SC_PWR_EN	GPIO3	GPIO3	SC_PWR_EN	SPI_CS0
A_4	SC_CLK_EN	GPIO4	GPIO4	SC_CLK_EN	SPI_CS1
A_5	SC_CARD_IN	GPIO5	GPIO5	SC_CARD_IN	SPI_CS2
A_6	UART_TX	IR_OUT	I2C_SCL	I2C_SCL	SPI_CS3
A_7	UART_RX	IR_IN	I2C_SDA	I2C_SDA	GPIO7

port.sel1.a	**7**	**8**	**9**	**10**	**11**
A_0	USR_RX_CLK_OUT	CNT1_TRIG	PWM1	PWM1	GPIO0
A_1	USR_TX_CLK_OUT	CNT2_TRIG	PWM2	PWM2	GPIO1
A_2	USR_DATA_OUT	CAP_TRIG1	CAP_TRIG1	CAP_TRIG1	GPIO2
A_3	USR_DATA0_IN	CAP_TRIG2	CNT1_TRIG	CAP_TRIG2	GPIO3
A_4	USR_DATA1_IN	CAP_TRIG3	CNT2_TRIG	CNT1_TRIG	GPIO4
A_5	USR_DATA2_IN	Reserved	Reserved	Reserved	GPIO5
A_6	USR_RX_CLK_IN	Reserved	Reserved	Reserved	GPIO6
A_7	USR_TX_CLK_IN	Reserved	Reserved	Reserved	GPIO7

Port B

port.sel1.b	**0**	**1**	**3**	**4**	**5**	**7**
B_0	GPIO8	SC_DATA_IN	SPI_SCLK	SC_DATA_IN	SC_DATA	USR_RX_CLK_OUT
B_1	GPIO9	SC_DATA_OUT	SPI_MOSI	SC_DATA_OUT	SC_RST	USR_TX_CLK_OUT
B_2	GPIO10	SC_RST	SPI_MISO	SC_RST	SC_PWR_EN	USR_DATA_OUT
B_3	GPIO11	SC_PWR_EN	GPIO8	SC_PWR_EN	SC_CLK_EN	USR_DATA0_IN
B_4	GPIO12	SC_CLK_EN	GPIO9	SC_CLK_EN	SC_CARD_IN	USR_DATA1_IN
B_5	Reserved	SC_CARD_IN	GPIO10	SC_CARD_IN	SPI_SCLK	USR_DATA2_IN
B_6	Reserved	IR_OUT	UART_TX	GPIO11	SPI_MOSI	USR_RX_CLK_IN
B_7	Reserved	IR_IN	UART_RX	GPIO12	SPI_MISO	USR_TX_CLK_IN

Port C

port.sel1.c	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
C_0	I2C_SCL	UART_TX	I2C_SCL	SPI_SCLK	I2C_SCL	UART_TX	IR_OUT	GPIO13
C_1	I2C_SDA	UART_RX	I2C_SDA	SPI_MOSI	I2C_SDA	UART_RX	IR_IN	GPIO14
C_2	UART_TX	IR_OUT	IR_OUT	SPI_MISO	GPIO15	GPIO15	GPIO15	GPIO15
C_3	UART_RX	IR_IN	IR_IN	GPIO16	GPIO16	GPIO16	GPIO16	GPIO16

Port D

port.sel1.d	**0**	**1**	**2**	**3**
D_0	WAKEUP	UARTB_RX	PWM1	WAKEUP
D_1	Reserved	UARTB_TX	PWM2	GPIO25
D_2	Reserved	GPIO21	UARTB_RX	GPIO27
D_3	Reserved	GPIO22	UARTB_TX	GPIO12

Port E

port.sel2.e	0	1	2	3
E_0	EMI_A0	HOST_D0	PIOA_0	GPIO0
E_1	EMI_A1	HOST_D1	PIOA_1	GPIO1
E_2	EMI_A2	HOST_D2	PIOA_2	GPIO2
E_3	EMI_A3	HOST_D3	PIOA_3	GPIO3
E_4	EMI_A4	HOST_D4	PIOA_4	GPIO4
E_5	EMI_A5	HOST_D5	PIOA_5	GPIO5
E_6	EMI_A6	HOST_D6	PIOA_6	GPIO6
E_7	EMI_A7	HOST_D7	PIOA_7	GPIO7

Port F

port.sel2.f	0	1	2	3
F_0	EMI_A8	HOST_D8	PIOA_8	GPIO8
F_1	EMI_A9	HOST_D9	PIOA_9	GPIO9
F_2	EMI_A10	HOST_D10	PIOA_10	GPIO10
F_3	EMI_A11	HOST_D11	PIOA_11	GPIO11
F_4	EMI_A12	HOST_D12	PIOA_12	GPIO12
F_5	EMI_A13	HOST_D13	PIOA_13	GPIO13
F_6	EMI_A14_DQM0	HOST_D14	PIOA_14	GPIO14
F_7	EMI_A15_DQM1	HOST_D15	PIOA_15	GPIO15

Port G

port.sel2.g	0	1	2	3
G_0	EMI_D0	HOST_D16	PWM1	Reserved
G_1	EMI_D1	HOST_D17	PWM2	Reserved
G_2	EMI_D2	HOST_D18	CNT1_TRIG	Reserved
G_3	EMI_D3	HOST_D19	CNT2_TRIG	GPIO25
G_4	EMI_D4	HOST_D20	CAP_TRIG1	UARTB_RX
G_5	EMI_D5	HOST_D21	CAP_TRIG2	UARTB_TX
G_6	EMI_D6	HOST_D22	CAP_TRIG3	GPIO21
G_7	EMI_D7	HOST_D23	CAP_TRIG4	GPIO22

Port H

port.sel2.h	0	1	3
H_0	EMI_D8_A16	HOST_D24	UARTB_RX
H_1	EMI_D9_A17	HOST_D25	UARTB_TX
H_2	EMI_D10_A18	HOST_D26	GPIO21
H_3	EMI_D11_A19	HOST_D27_A3	GPIO22
H_4	EMI_D12_A20	HOST_D28_A4	GPIO23
H_5	EMI_D13_A21	HOST_D29_A5	GPIO24
H_6	EMI_D14_A22	HOST_D30_A6	GPIO25
H_7	EMI_D15_A23	HOST_D31_A7	GPIO26

Port I

port.sel3.i	**0**	**1**	**2**	**3**
I_0	EMI_CS0	HOST_REQ	CNT1_TRIG	UARTA_RX
I_1	EMI_CS1	HOST_ACK	CNT2_TRIG	UARTA_TX
I_2	EMI_DS1_WS1_RAS	HOST_RW	CAP_TRIG1	GPIO17
I_3	EMI_DS0_WS0_CAS	HOST_CS	CAP_TRIG2	GPIO18
I_4	EMI_RW_RS_WEN	HOST_WAIT	CAP_TRIG3	GPIO19
I_5	EMI_CKE	HOST_A0	CAP_TRIG4	GPIO20
I_6	EMI_WAIT	HOST_A1	CAP_TRIG5	GPIO25
I_7	EMI_CLK	HOST_A2	CAP_TRIG6	GPIO26

Port J

port.sel3.j	**0**	**2**	**3**
J_0	UARTA_RX	UARTA_RX	UARTA_RX
J_1	UARTA_TX	UARTA_TX	UARTA_TX
J_2	GPIO17	GPIO27	GPIO17
J_3	GPIO18	GPIO28	GPIO18
J_4	UARTB_RX	UARTB_RX	GPIO19
J_5	UARTB_TX	UARTB_TX	GPIO20
J_6	GPIO21	PWM1	PWM1
J_7	GPIO22	PWM2	PWM2

Port K

port.sel3.k	**1**	**2**	**3**	**4**
K_0	CNT1_TRIG	PIOB_0	GPIO0	UARTB_RX
K_1	CNT2_TRIG	PIOB_1	GPIO1	UARTB_TX
K_2	CAP_TRIG1	PIOB_2	GPIO2	GPIO21
K_3	CAP_TRIG2	PIOB_3	GPIO3	GPIO22
K_4	CAP_TRIG3	PIOB_4	GPIO4	GPIO23
K_5	CAP_TRIG4	PIOB_5	GPIO5	GPIO24
K_6	PWM1	PIOB_6	PWM1	GPIO26
K_7	PWM2	PIOB_7	PWM2	GPIO27

Port L

port.sel2.l	**1**	**2**	**3**
L_0	PIOB_8	GPIO8	CNT1_TRIG
L_1	PIOB_9	GPIO9	CNT2_TRIG
L_2	PIOB_10	GPIO10	CAP_TRIG1
L_3	PIOB_11	GPIO11	CAP_TRIG2
L_4	PIOB_12	GPIO12	CAP_TRIG3
L_5	PIOB_13	GPIO13	CAP_TRIG4
L_6	PIOB_14	GPIO14	CAP_TRIG5
L_7	PIOB_15	GPIO15	CAP_TRIG6

Peripheral Routing Options

The eCOG1k device pins are connected to 12 I/O ports labelled A to L. Different peripheral functions can be mapped to these ports to define the operation of each pin. This section lists the available routing options for each peripheral function. For further information on configuring the I/O ports, see the eCOG1k User Manual.

GPIO

Peripheral	Signals	Ports	
GPIO	GPIO0-7	A_0-7	E_0-7
	GPIO0-5	K_0-5	
	GPIO3-5	A_3-5	
	GPIO7	A_7	
	GPIO8-15	F_0-7	L_0-7
	GPIO8-12	B_0-4	
	GPIO8-10	B_3-5	
	GPIO11-12	B_6-7	
	GPIO13-16	C_0-3	
	GPIO15-16	C_2-3	
	GPIO16	C_3	
	GPIO17-20,25,26	I_2-7	
	GPIO17,18,21,22	J_2-3,6-7	
	GPIO17-20	J_2-5	
	GPIO21-22	D_2-3	
	GPIO21-26	H_2-7	
	GPIO21-24,26-27	K_2-7	
	GPIO25,27,12	D_1-3	
	GPIO25,21,22	G_3,6-7	
	GPIO27-28	J_6-7	

PIO

Peripheral	Signals	Ports
PIOA	PIOA_0-7	E_0-7
	PIOA_8-15	F_0-7
PIOB	PIOB_0-7	K_0-7
	PIOB_8-15	L_0-7

DUART

Peripheral	Signals	Ports					
UARTA	UARTA_RX	I_0	J_0				
	UARTA_TX	I_1	J_1				
UARTB	UARTB_RX	D_0	D_2	G_4	H_0	J_4	K_0
	UARTB_TX	D_1	D_3	G_5	H_1	J_5	K_1

DUSART

The routing options for the DUSART peripheral functions are listed in the tables below.

UART

Peripheral	Signals	Ports			
UART	UART_TX	A_6	B_6	C_0	C_2
	UART_RX	A_7	B_7	C_1	C_3

SPI

Peripheral	Signals	Ports			
SPI	SPI_SCLK	A_0	B_0	B_5	C_0
	SPI_MOSI	A_1	B_1	B_6	C_1
	SPI_MISO	A_2	B_2	B_7	C_2
	SPI_CS0	A_3			
	SPI_CS1	A_4			
	SPI_CS2	A_5			
	SPI_CS3	A_6			

I^{2}C

Peripheral	Signals	Ports	
I^{2}C	I2C_SCL	A_6	C_0
	I2C_SDA	A_7	C_1

Smart Card Interface (SCI)

Peripheral	Signals	Ports		
SCI	SC_DATA			B_0
	SC_DATA_IN	A_0	B_0	
	SC_DATA_OUT	A_1	B_1	
	SC_RESET	A_2	B_2	B_1
	SC_PWR_EN	A_3	B_3	B_2
	SC_CLK_EN	A_4	B_4	B_3
	SC_CARD_IN	A_5	B_5	B_4

Infra Red (IFR)

Peripheral	Signals	Ports			
IR	IR_OUT	A_6	B_6	C_0	C_2
	IR_IN	A_7	B_7	C_1	C_3

User Serial Port (USR)

Peripheral	Signals	Ports
USRA	USRA_RX_CLK_OUT	B_0
	USRA_TX_CLK_OUT	B_1
	USRA_DATA_OUT	B_2
	USRA_DATA0_IN	B_3
	USRA_DATA1_IN	B_4
	USRA_DATA2_IN	B_5
	USRA_RX_CLK_IN	B_6
	USRA_TX_CLK_IN	B_7
USRB	USRB_RX_CLK_OUT	A_0
	USRB_TX_CLK_OUT	A_1
	USRB_DATA_OUT	A_2
	USRB_DATA0_IN	A_3
	USRB_DATA1_IN	A_4
	USRB_DATA2_IN	A_5
	USRB_RX_CLK_IN	A_6
	USRB_TX_CLK_IN	A_7

Timers

Peripheral	Signals	Ports						
CNT1	CNT1_TRIG	A_0	A_3	A_4	G_2	I_0	K_0	L_0
CNT2	CNT2_TRIG	A_1	A_4		G_3	I_1	K_1	L_1
PWM1	PWM1	A_0	D_0		G_0	J_6	K_6	
PWM2	PWM2	A_1	D_1		G_1	J_7	K_7	
CAP	CAP_TRIG1	A_2						
	CAP_TRIG1-2	A_2-3						
	CAP_TRIG1-3	A_2-4						
	CAP_TRIG1-4	G_4-7	K_2-5					
	CAP_TRIG1-6	I_2-7	L_2-7					

External Memory Interface (EMI)

Peripheral	Signals	Ports
EMI	EMI_D0-D7	G_0-7
	EMI_D8-15/A16-A23	H_0-7
	EMI_A0-A7	E_0-7
	EMI_A8-11	F_0-3
	EMI_A12-13 EMI_A14_DQML EMI_A15_DQMH	F_4-5 F_6 F_7
	EMI_CS0	I_0
	EMI_CS1	I_1
	EMI_DS1_WS1_RAS	I_2
	EMI_DS0_WS0_CAS	I_3
	EMI_RW_RS_WEN	I_4
	EMI_CKE	I_5
	EMI_WAIT	I_6
	EMI_CLK	I_7

External Host Interface (EHI)

Peripheral	Signals	Ports
EHI	HOST_D0-7	E_0-7
	HOST_D8-15	F_0-7
	HOST_D16-23	G_0-7
	HOST_D24-26 HOST_D27-31/A3-7	H_0-2 H_3-7
	HOST_REQ	I_0
	HOST_ACK	I_1
	HOST_RW	I_2
	HOST_CS	I_3
	HOST_WAIT	I_4
	HOST_A0-2	I_5-7

Analogue Inputs

The ADC peripheral input signals are dedicated and are not controlled by the port multiplexer.

Applications Information

Connections

For normal operation, the following recommendations should be observed in the hardware design.

- The TEST and CPU_Break pins are not used in normal applications and should be connected to GND, either directly or via 1k pull-down resistors.
- The MODE pin is connected to V_{DD} for the eCOG1k and to GND for the eCOG1i.
  It is possible to fit an eCOG1i device in hardware designed for the eCOG1k with certain restrictions; please refer to Technical Note TN001 for more details.
- The eICE_LOADB pin must be connected to V_{DD} via a 100kΩ pull-up resistor for normal operation when the eICE debug port is not in use or disconnected. When the eICE port is used for debugging, a 4.7kΩ pull-up resistor is required. If the system is used with an external eICE programming adaptor, then the external adaptor has the 4.7kΩ pull-up resistor fitted, and the target system only needs a 100kΩ pull-up resistor connected to this signal.
  It is also recommended that the eICE input signals (eICE_CLK, eICE_MOSI, eICE_CS) are connected to GND via 100kΩ pull-down resistors as a precaution against noise.
- The external quartz crystal used with the 5MHz high reference oscillator requires two load capacitors. The maximum load capacitance value for the high reference oscillator is 32pF, including any package and stray capacitance due to the circuit board layout. The recommended load capacitor value is 18pF. Higher load capacitor values increase slightly the power consumption of the oscillator circuit.

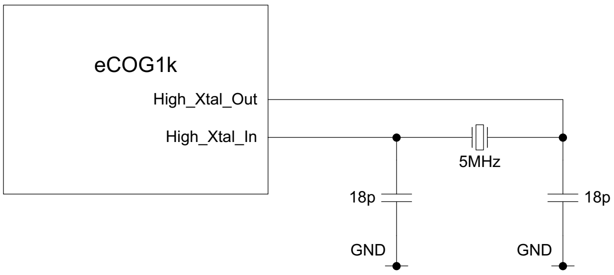


Figure 2: High reference oscillator external components

- If an external clock source is used instead of the 5 MHz quartz crystal oscillator, then the High_XTAL_Out pin is not connected and the external clock signal is connected to High_XTAL_In through a 100pF series coupling capacitor.
  If the high speed clock is not required, then High_XTAL_Out is not connected and High_XTAL_In is connected to V_{DD} via a 10kΩ pull-up resistor.
- The external quartz crystal used with the 32.768kHz low reference oscillator requires two load capacitors. The maximum load capacitance value for the low reference oscillator is 25pF, including any package and stray capacitance due to the circuit board layout. The recommended load capacitor value is 10pF. Higher load capacitor values increase slightly the power consumption of the oscillator circuit.

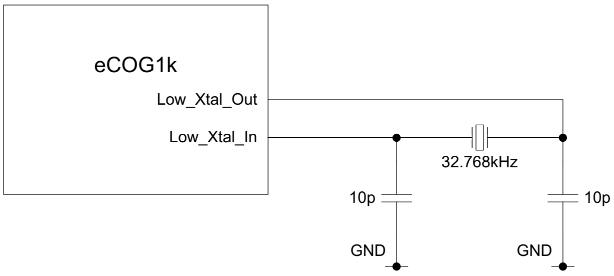


Figure 3: Low reference oscillator external components

- If an external clock source is used instead of the 32.768 kHz quartz crystal oscillator, then the Low_XTAL_Out pin is not connected and the external clock signal is connected directly to Low_XTAL_In. No coupling capacitor is required.
  If the low speed clock is not required, then Low_XTAL_Out is not connected and Low_XTAL_In is connected to V_{DD} via a 10kΩ pull-up resistor.

- The Reset_Out and Reset_In pins are not connected internally. This allows the use of an external reset circuit if required. A power-on reset signal must be connected to Reset_In for correct operation of the device, either from the internal reset circuit or from an external power-on reset circuit. To use the internal power-on reset circuit, connect Reset_Out to Reset_In, either directly or (as on the eCOG1k development boards) via external logic for any additional external reset source such as a pushbutton switch. Reset_In has a Schmitt trigger input circuit.
- NC indicates a No Connect. Any pins labelled as NC should not be connected in circuit.
- All digital input pins and bidirectional port pins have Schmitt trigger input circuits.

For low power operation, note the following additional recommendations.

- The EMI data bus pins float as inputs in the sleep state and can cause higher than expected power consumption. If minimum power consumption in the sleep state is required, connect all the EMI data bus pins to GND or to V_{DD} via 100kΩ resistors.
- Similarly, all unused port input pins should be connected to GND or to V_{DD} via 100kΩ resistors to prevent them floating.

Power Supplies and Decoupling

It is recommended that V_{DD} and GND are implemented as power and ground planes in the printed circuit board. The analogue power supply connections to the AV_{DD} and AGND pins should be routed directly to separate power and ground planes, they should not share circuit tracks with any of the digital power supply connections. An ideal board layout should provide split power and ground plane areas to separate the digital and analogue power supplies.

Decoupling capacitors must be fitted on both the digital and analogue power supplies. The digital power supply connections should have at least one 100nF capacitor for every two power pins, located close to these pins. Ideally there should be one decoupling capacitor for each power pin, using both 10nF and 100nF values. The analogue power supply should be decoupled separately with both a 100nF and a 1nF capacitor in parallel, located as close as possible to the AV_{DD} and AGND pins. All these decoupling capacitors should be low ESR ceramic types.

Additional bulk decoupling is required somewhere on the hardware design. At least one 10uF low ESR tantalum or aluminium electrolytic capacitor is required on each power supply, usually located at the power supply input connections or at the output of any power supply regulator. For larger designs it is recommended that multiple capacitors are fitted; these should be distributed around the circuit board.

For further filtering on the analogue power supply, connect a ferrite bead in series with the analogue supply input, in between the power plane and the decoupling capacitors. A suitable surface mount ferrite bead is the EPCOS B82496C3100J (inductance 10nH, 500mA, 0.3Ω DC resistance, 0603 package) available from Farnell Electronic Components (order number 387-7024).

If the cost of a multilayer circuit board is too high for the target system and the layout is implemented without power and ground planes, then care must be taken to minimise the series impedance in the power and ground connections. Keep the power and ground tracks as short and as wide as possible, and locate the decoupling capacitors as close as possible to the package power pins. Route separate power and ground tracks from the power supply input connection to the ferrite bead and then to the decoupling capacitors for the analogue power and ground pins AV_{DD} and AGND, and make sure that the decoupling capacitors are located as close as possible to these pins.

Electrical Characteristics

Recommended Operating Conditions

Except where otherwise specified, eCOG1k meets all operating specifications when operated within these limits.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_A	Operating Temperature		–40		+85	°C
V_{DD}	Digital Supply Voltage	Relative to GND	3.0	3.3	3.6	V
AV_{DD}	Analogue Supply Voltage	Relative to GND	3.0	3.3	3.6	V
V_{IN}	Voltage on any pin	Relative to GND	–0.5		V_{DD} + 0.3	V

Table 7: Recommended operating conditions

Absolute Maximum Ratings

The eCOG1k device is not guaranteed to meet specification if it is operated outside the recommended operating conditions. In addition, exceeding these maximum operating parameters may cause permanent damage to the device.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_A	Operating Temperature		–40		+105	°C
V_{DD}	Digital Supply Voltage	Relative to GND	–0.5		3.7	V
AV_{DD}	Analogue Supply Voltage	Relative to GND	–0.5		3.7	V
V_{IN}	Voltage on any pin	Relative to GND	–0.5		3.7	V
V_{ESD}	ESD Protection	Human Body Model			2	kV
		Charge Device Model			500	V

Table 8: Absolute maximum ratings

Supply Current

Executing from Flash

The following table lists the minimum supply current for the eCOG1k in all possible clock source configurations, with the CPU executing code from internal flash memory and all peripherals disabled. The CPU is set to run at the maximum clock frequency for each configuration.

Symbol	Configuration	Clocks Enabled	CPU Clock	Min	Typ	Max	Units
I_{CPU6}	All clocks	low ref + low PLL + high ref + high PLL	25MHz †		17.3		mA
I_{CPU5}	High PLL + stepup	low ref + low PLL + high PLL	24.576MHz †		17.2		mA
I_{CPU4}	Hgh PLL	low ref + high ref + high PLL	25MHz †		17.0		mA
I_{CPU3}	Low PLL	low ref + low PLL	2.4576MHz		3.5		mA
I_{CPU2}	High ref osc.	low ref + high ref	2.5MHz		3.4		mA
I_{CPU1}	Low ref osc.	low ref	16kHz		1.9		mA
I_{SLEEP}	Sleep mode	low ref			4		μA

Table 9: Supply current (executing from flash, zero wait states)

† At CPU clock frequencies above 10MHz, the internal flash memory is set to use one wait state. Below 10MHz CPU clock, the internal flash operates at zero wait states.

Executing from Cache with Wait States

The following table lists the minimum supply current for the eCOG1k in all possible clock source configurations, with the CPU executing code from the internal instruction cache and all peripherals disabled. The CPU is set to run at the maximum clock frequency for each configuration. The cache wait states are set to give the same read performance as the internal flash.

Symbol	Configuration	Clocks Enabled	CPU Clock	Min	Typ	Max	Units
I_{CPU6}	All clocks	low ref + low PLL + high ref + high PLL	25MHz †		14.3		mA
I_{CPU5}	High PLL + stepup	low ref + low PLL + high PLL	24.576MHz †		14.2		mA
I_{CPU4}	Hgh PLL	low ref + high ref + high PLL	25MHz †		14.0		mA
I_{CPU3}	Low PLL	low ref + low PLL	2.4576MHz		1.55		mA
I_{CPU2}	High ref osc.	low ref + high ref	2.5MHz		1.40		mA
I_{CPU1}	Low ref osc.	low ref	16kHz		11		μA
I_{SLEEP}	Sleep mode	low ref			4		μA

Table 10: Supply current (executing from cache with wait states)

† At CPU clock frequencies above 10MHz, the internal flash memory is set to use one wait state and the supply current is measured with the cache set to three wait states. At CPU clock frequencies below 10MHz, the internal flash operates at zero wait states and the supply current is measured with the cache set to two wait states.

Executing from the instruction cache instead of internal flash memory normally increases the CPU execution speed and therefore the supply current, because instruction fetches from cache are faster than from internal flash. The values in the table above are measured with cache wait states set to keep the same instruction execution speed as when executing from flash memory, to avoid increasing the supply current due to the increased execution speed.

Executing code continuously from the instruction cache rather than from internal flash memory reduces the supply current by approximately 2mA at CPU clock frequencies below 10MHz, and by 2.8mA at a CPU clock frequency of 25MHz, when the cache is set to use wait states such that the execution speed is not increased.

Executing from Cache at Full Speed

The following table lists the minimum supply current for the eCOG1k in all possible clock source configurations, with the CPU executing code from the internal instruction cache and all peripherals disabled. The CPU is set to run at the maximum clock frequency for each configuration. The cache wait states are set to zero for maximum performance.

Symbol	Configuration	Clocks Enabled	CPU Clock	Min	Typ	Max	Units
I_{CPU6}	All clocks	low ref + low PLL + high ref + high PLL	25MHz		21.5		mA
I_{CPU5}	High PLL + stepup	low ref + low PLL + high PLL	24.576MHz		21.4		mA
I_{CPU4}	Hgh PLL	low ref + high ref + high PLL	25MHz		21.0		mA
I_{CPU3}	Low PLL	low ref + low PLL	2.4576MHz		2.18		mA
I_{CPU2}	High ref osc.	low ref + high ref	2.5MHz		2.06		mA
I_{CPU1}	Low ref osc.	low ref	16kHz		16		μA
I_{SLEEP}	Sleep mode	low ref			4		μA

Table 11: Supply current (executing from cache, zero wait states)

Executing from the instruction cache instead of internal flash memory increases the CPU execution speed at clock frequencies above 10MHz, because instruction fetches from flash require at least one wait state and instruction fetches from cache do not. This also increases the supply current when executing from cache at these higher clock frequencies. At clock frequencies below 10MHz, there is no difference in execution speed when reading code from cache or from flash, and executing from cache reduces the supply current.

Sleep Mode

The following table lists the supply current for the eCOG1k in all possible clock source configurations, with the CPU in sleep mode and all peripherals disabled. This shows the supply current for the clock oscillators and PLL multipliers.

Symbol	Configuration	Clocks Enabled	Min	Typ	Max	Units
I_{CK6}	All clocks	low ref + low PLL + high ref + high PLL		2.15		mA
I_{CK5}	High PLL + stepup	low ref + low PLL + high PLL		2.06		mA
I_{CK4}	High PLL	low ref + high ref + high PLL		1.90		mA
I_{CK3}	Low PLL	low ref + low PLL		260		μA
I_{CK2}	High ref oscillator	low ref + high ref		102		μA
I_{CK1}	Low ref oscillator	low ref		4		μA

Table 12: Supply current (sleep mode)

DC Electrical Characteristics

Digital Inputs and Outputs

$3.0V \leq V_{DD} \leq 3.6V$

Symbol	Parameter	Conditions	Min	Max	Units
	Inputs [1]				
V_{IL}	Input Low Voltage		–0.3	+0.8	V
V_{IH}	Input High Voltage		0.7 x V_{DD}	V_{DD} + 0.3	V
I_{OZ}	Input leakage current	GND – 0.3V≤ V_{IN} ≤ V_{DD} + 0.3V	–5	5	µA
C_{IN}	Input capacitance			4.5	pF
	2mA outputs [2]				
V_{OL}	Output Low Voltage	I_{OL} = 2mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –2mA	V_{DD} – 0.4		V
I_{OL}	Logic Low Output Current	V_{OL} < 0.4V	2		mA
I_{OH}	Logic High Output Current	V_{OH} > V_{DD} – 0.4V	–2		mA
	4mA outputs [3]				
V_{OL}	Output Low Voltage	I_{OL} = 4mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	V_{DD} – 0.4		V
I_{OL}	Logic Low Output Current	V_{OL} < 0.4V	4		mA
I_{OH}	Logic High Output Current	V_{OH} > V_{DD} – 0.4V	–4		mA
	8mA outputs [4]				
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –8mA	V_{DD} – 0.4		V
I_{OL}	Logic Low Output Current	V_{OL} < 0.4V	8		mA
I_{OH}	Logic High Output Current	V_{OH} > V_{DD} – 0.4V	–8		mA

Table 13: DC electrical characteristics - digital inputs and outputs

[1] All digital input pins and bidirectional port pins have Schmitt trigger input circuits.

[2] The following pins have 2mA output drive capability:
eICE_MISO, eICE_LOADB, RESET_OUT, PORTA_0-7, PORTB_0-7, PORTC_0-3, PORTD_0-3, PORTJ_0-7

[3] The following pins have 4mA output drive capability:
PORTE_0-7, PORTF_0-7, PORTG_0-7, PORTH_0-7, PORTI_0-7, PORTL_0-7

[4] The following pins have 8mA output drive capability:
PORTK_0-7

Analogue Inputs

$AV_{DD} = 3.3V$

Symbol	Parameter	Conditions	Min	Max	Units
V_{IN}	Input Voltage Range		0.20	2.66	V
V_{ICM}	Input Common Mode Voltage Range		0.20	2.66	V
V_{DIFF}	Input Voltage Difference		–1.3	1.3	V
C_{INA}	Input Capacitance (each input to ground)			4.5	pF

Table 14: DC electrical characteristics - analogue inputs

AC Electrical Characteristics

All signal timing information is given for output pin load capacitances of 30pF, unless specified otherwise.

Crystal Oscillators

This table lists the performance characteristics of the low and high frequency oscillators over the full range of process variation and supply voltage.
$3.0V \le AV_{DD} \le 3.6V$, $T_A = 25°C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Low Reference Oscillator					
F_{32k}	Operating frequency (32.768kHz crystal)	Combined crystal tolerance is ±150ppm worst case.	32.763	32.768	32.773	kHz
C_{32k}	Duty cycle	F_{32k} = 32.768kHz	45	50	55	%
T_{SCV}	Time from start to valid clock signal	C_L = 12.5pF, C_O = 1.5pF ESR_{MAX} = 30kΩ		400		ms
T_{SSA}	Time from start to stable amplitude			500	600	ms
C_L	Load capacitor value			10	25	pF
	High Reference Oscillator					
F_{5M}	Operating frequency (5.0MHz crystal)	Combined crystal tolerance is ±50ppm worst case.	4.99975	5.000	5.00025	MHz
F_{HR}	Frequency range	With appropriate crystal.	4	5.0	10	MHz
C_{5M}	Duty cycle	F_{5M} = 5MHz	45	50	55	%
T_{SCV1}	Time from start to valid clock signal	C_L = 12.0pF, C_O = 1.5pF ESR_{MAX} = 150Ω		1	2	ms
T_{SCV2}		C_L = 32.0pF, C_O = 9pF ESR_{MAX} = 150Ω		12	15	ms
C_L	Load capacitor value			18	32	pF

Table 15: AC characteristics - crystal oscillators

The crystal oscillator circuits require external load capacitors connected from both ends of the quartz crystal to GND, as shown in Applications Information. The recommended load capacitor values are 10pF for the low reference oscillator and 18pF for the high reference oscillator.

Phase Locked Loops (PLLs)

This table lists the performance characteristics of the low and high frequency phase locked loops over the full range of process variation and supply voltage.
$3.0V \le AV_{DD} \le 3.6V$, $T_A = 25°C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Low PLL					
F_{LK}	Lock range		16		55	kHz
	High PLL					
F_{LK}	Lock range		1.5		11	MHz

Table 16: AC characteristics - PLLs

External Clock Source

If an external clock source is used as the main system clock for the eCOG1k, the following parameters apply.

$3.0V \le AV_{DD} \le 3.6V$, $T_A = 25°C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Low reference clock input					
F_{LO}	Input frequency				10	MHz
	High reference clock input					
F_{HI}	Input frequency				>30	MHz
	Input signal parameters					
t_{CKH}	Clock high time	Clock at 90% of V_{DD} or more	10			ns
t_{CKL}	Clock low time	Clock at 10% of V_{DD} or less	10			ns
t_R	Clock rise time	10% to 90%			100	ns
t_F	Clock fall time	90% to 10%			100	ns

Table 17: AC characteristics - external clock source

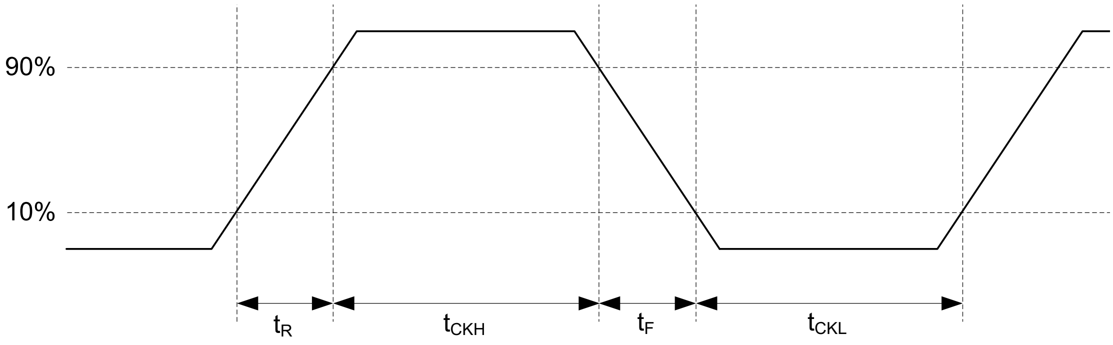


Figure 4: External clock source timing diagram

Digital Inputs

The input pulse width specification applies to any input signal which is sampled by a peripheral of the chip. All inputs are clocked through synchroniser circuits to eliminate metastable data when reading input registers.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Inputs					
T_{Pmin}	Minimum pulse width	Peripheral sample clock period is T_S, determined by peripheral clock configuration.	$3T_S$			sec

Table 18: AC characteristics - digital inputs

Embedded Flash Memory Characteristics

$3.0V \leq V_{DD} \leq 3.6V$, $0°C \leq T_A \leq 85°C$.

Symbol	Parameter	Min	Typ	Max	Units
	Read operation				
T_{RD}	Read access time			45	ns
T_{CY}	Read cycle time			100	ns
I_{FR}	Read current (continuous read)			20	mA
I_{FS}	Read standby current			10	µA
	Program/erase operation				
T_{PE}	Page erase time	10			ms
T_{CE}	Chip erase time	200			ms
T_{WP}	Word programming time	20			µs
T_{HV}	Cumulative programming duration of each page between erase operations.			4	ms
N_{EP}	Maximum erase/program cycles	$20x10^3$	$200x10^3$		cycles
T_{DR}	Data retention time	100			years
I_{FP}	Active program current			10	mA
I_{FE}	Active erase current			7	mA

Table 19: Embedded flash memory characteristics

Analogue Characteristics

ADC

The ADC measures the difference between two analogue input signals, depending on the selected configuration of the ADC input multiplexer.

The conversion span of the ADC is determined by the internal reference voltage V_{REF}, nominally 1.25V. The difference between the positive and negative input voltages is calculated from the ADC output value *R* according to the following equation:

$$V_A - V_B = \left(\frac{R \times V_{REF}}{2048}\right)$$

The expected ADC output value *R* is calculated from the difference between the positive and negative input voltages according to the following equation:

$$R = \left(\frac{V_A - V_B}{V_{REF}}\right) \times 2048$$

At AV_{DD} = 3.3V, clock frequency = 512kHz, input frequency = 999Hz, noise bandwidth:1Hz to 4kHz, input signal –3dBFS, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Dynamic Performance					
SNR	Signal to Noise Ratio without Harmonics			62		dB
DR	Dynamic Range			65		dB
THD	Total Harmonic Distortion			–60		dB
	Static Performance					
	Linearity	-40°C ≤ T_A ≤ 105°C		±0.05	±0.2	%
	Accuracy	-40°C ≤ T_A ≤ 105°C		±0.5	±2.0	%
V_{REF}	Reference Voltage	-40°C ≤ T_A ≤ 105°C	1.24	1.25	1.26	V
V_{CM}	Common-Mode Signal Reference Voltage	-40°C ≤ T_A ≤ 105°C	1.42	1.43	1.44	V
V_{SPAN}	Conversion range	Modes A and B	$V_{IN} = V_{CM} \pm V_{REF}$			V
		Modes C and D	$\lvert(V_{INA} - V_{INB})\rvert \le V_{REF}$			V
	Analogue Inputs					
V_{IN}	Input Voltage Range		0.20		2.66	V
V_{ICM}	Common Mode Input Voltage Range		0.20		2.66	V
V_{DIFF}	Input Voltage Difference		–1.3		1.3	V
C_{INA}	Input Capacitance (each input to ground)				4.5	pF
	Switching Performance					
T_{STABLE}	First conversion after module is activated	First sample arrives at the sample rate plus a settling time.			5	μs
T_{MUX}	Data latency after changing multiplexer channel	Equal to four sample times			0.5	ms

Table 20: ADC characteristics

Temperature Sensor

The temperature sensor generates a voltage proportional to absolute temperature, in addition to temperature stable reference voltages which are used by the ADC converter. Actual temperature is calculated from the ADC value *R* using the following equation:

$$T_A = T_{CAL} + (R \times 0.061)$$

where T_{CAL} is the calibration offset for the device.

The expected ADC output value *R* is calculated from the ambient temperature according to the following equation:

$$R = \left(\frac{T_A - T_{CAL}}{0.061}\right)$$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_A	Ambient Temperature		-40		+105	°C
T_{CAL}	Calibration Offset	-40°C ≤ T_A ≤ 105°C AV_{DD} = 3.3V		6.9		°C
T_{ERR}	Temperature accuracy after offset calibration	-40°C ≤ T_A ≤ 105°C AV_{DD} = 3.3V		±0.2	±2.0	°C
T_{START}	Start Up Time	After the module is activated		35	40	μs

Table 21: Temperature sensor characteristics

Supply Voltage Sensor

The supply voltage sensor generates a voltage equal to (AV_{DD} – AGND) / 6 from a resistive divider, which is connected to the differential inputs of the ADC converter when selected. The supply voltage is calculated from the ADC value *R* using the following equation:

$$AV_{DD} = \left(\frac{R \times V_{REF}}{2048}\right) \times K_V$$

where K_V is the division factor for the voltage divider chain, nominally 6.0.

The expected ADC output value *R* is calculated from the analogue power supply voltage according to the following equation:

$$R = \left(\frac{AV_{DD} \times 2048}{K_V \times V_{REF}}\right)$$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AV_{DD}	Supply Voltage		2.7		3.6	V
K_V	Division factor	-40°C ≤ T_A ≤ 105°C	5.7	6.0	6.3	
V_{ERR}	Voltage accuracy	T_A = 25°C		±0.05	±0.1	V
		-40°C ≤ T_A ≤ 105°C			±0.2	V

Table 22: Supply voltage sensor characteristics

Power-On Reset

The eCOG1k has an internal supply voltage sense circuit used for the power-on reset function. It is designed for use with nominal power supply voltages between 3.0 and 3.6V and provides a reset indication when the supply voltage is below 2.7V.

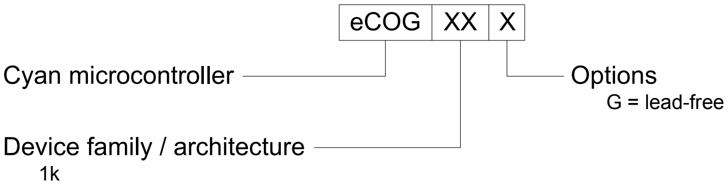
Symbol	Parameter	Conditions	Min	Typ	Max	Units
AV_{DD}	Supply voltage		1.7	3.3	3.6	V
V_{OUT}	Voltage on Reset_Out	Reset True (Asserted)		AV_{DD}		V
V_{TH+}	Threshold Voltage	AV_{DD} rising	2.60	2.72	2.91	V
V_{TH-}	Threshold Voltage	AV_{DD} falling	2.55	2.67	2.86	V
ΔV	Hysteresis			50		mV
T_{POR}	Reset Output Time		6.8			µs
T_{RH}	Internal reset hold time	F_{32k} = 32.768 kHz			64	T_{CLK_32k}
		F_{5M} = 5 MHz			1024	T_{CLK_5M}

Table 23: Power-on reset characteristics

The power-on reset circuit output signal is available on the Reset_Out pin, and is active high. In normal use this is connected to the Reset_In pin, either directly or via any external logic to support additional reset input signals from a user pushbutton or hardware watchdog.

Each reference clock input has a "clock valid" detector circuit, triggered after four valid clock transitions. The clock inputs can be selected for use only when their clock valid signal is asserted. Each reference clock also feeds into a ripple counter, 64 clocks for the low reference input and 1024 clocks for the high reference input. For each of the two clock inputs, once a valid clock is detected, the system is held in reset until these two ripple counters reach their terminal count. This guarantees that reset is not released until the connected crystal oscillators are running and with the normal crystal frequencies provides a 3ms reset hold time.

Part Number Description



Ordering Information

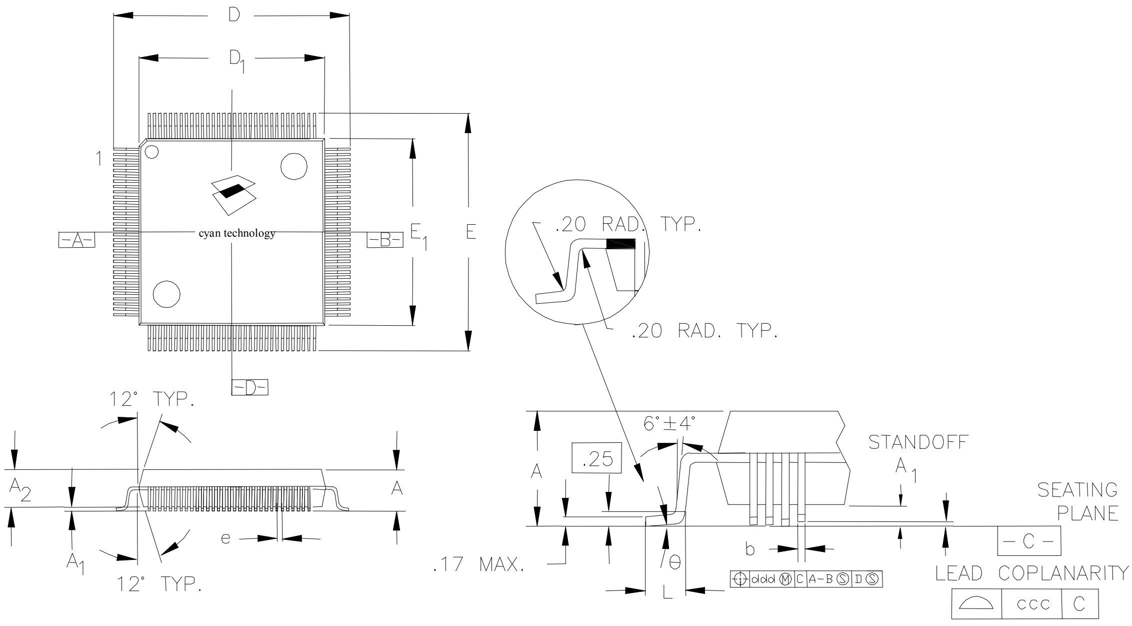
Part number	Flash size	ADC	I/Os	Package
eCOG1kG	64K	4	88	128TQFP (lead-free)

Table 24: eCOG1k Ordering Information

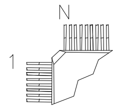
Mechanical Package Drawing

128TQFP

The eCOG1kG is available in a 128 pin TQFP package.
Pin pitch 0.4mm, 14x14mm body, 16x16mm at pin edge.



ANOTHER VARIATION OF PIN 1 VISUAL AID

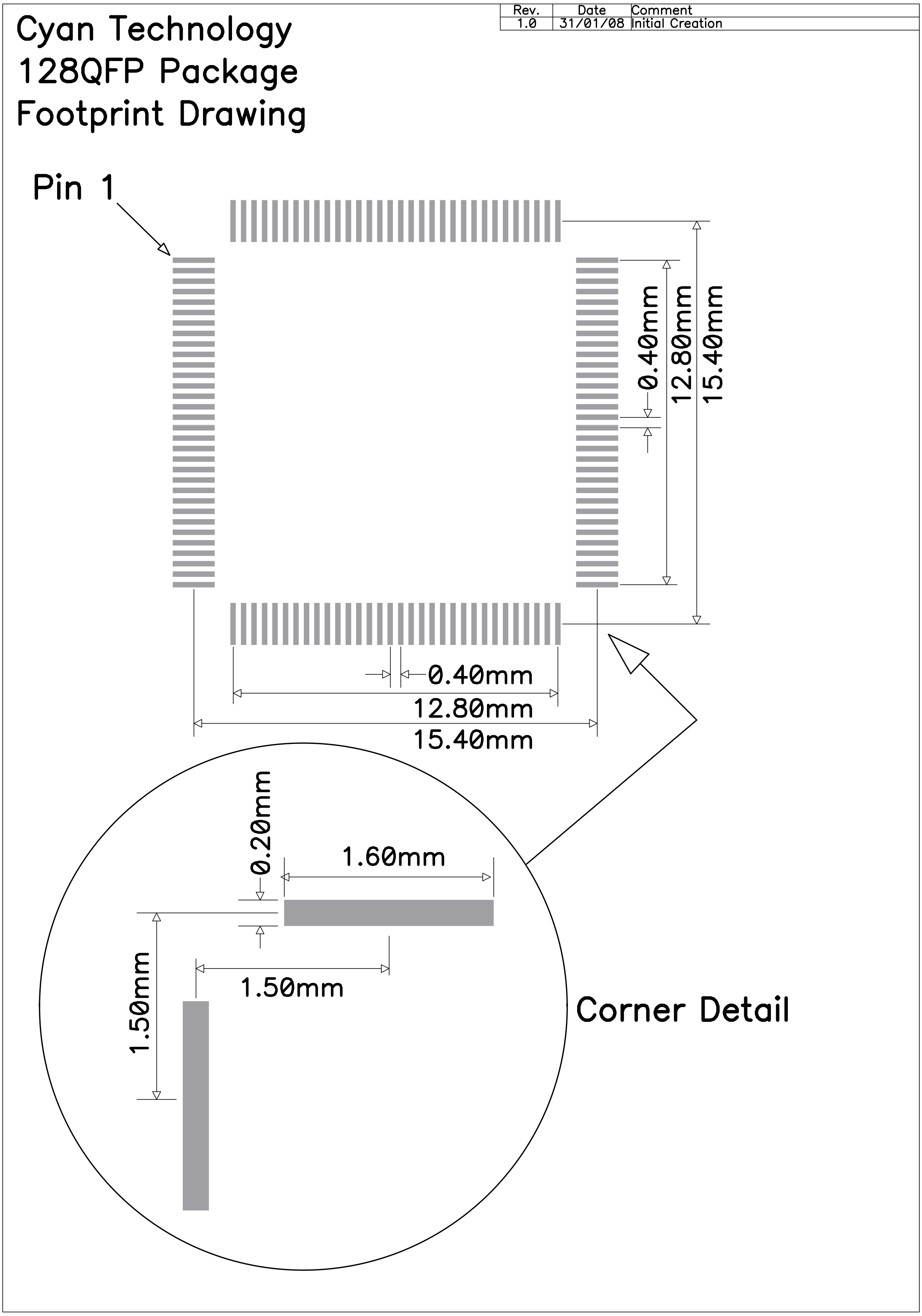


BODY + 2.00 mm FOOTPRINT			
	LEADS	128L 1.4 THK	
DIMS.	TOL. L/F	.127	.152
A	MAX.	1.60	
A_1	.05 MIN./.15 MAX.		
A_2	±.05	1.40	
D	±.20	16.00	
D_1	±.05	14.00	
E	±.20	16.00	
E_1	±.05	14.00	
L	+.15/-.10	.60	
e	BASIC	.40	
b	±.05	.18	
θ	0°-7°		
ddd	MAX.	.07	
ccc	MAX.	.08	

NOTES:
1) ALL DIMENSIONS IN MM.
2) DIMENSIONS SHOWN ARE NOMINAL WITH TOL. AS INDICATED.
3) L/F: EFTEC 64T COPPER OR EQUIVALENT, 0.127 MM (.005") OR 0.15 MM (.006") THICK.
4) FOOT LENGTH "L" IS MEASURED AT GAGE PLANE, AT 0.25 ABOVE THE SEATING PLANE.

Circuit Board Pad Layout Drawings

128TQFP



Notes

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I2C and the I2C interface are patented by Philips Semiconductor in certain territories.

Philips may demand a royalty or licence fee from designs using the I2C interface.

Declaration of RoHS Compliance

Cyan Technology Ltd hereby declares that the eCOG1kG is in full compliance with the European Directive 2002/95/EC, The Restriction of Hazardous Substances in Electrical and Electronic Equipment (RoHS).

This declaration is made based on data provided by our material suppliers, and independent analysis of all homogenous materials used in the manufacture of the product.

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